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LIGHT OUTPUT CONTROL CIRCUIT

BACKGROUND OF THE INVENTION

5 1. Field of the Invention

The present invention relates to a light output control circuit for controlling the light output of a light-emitting device, such as a semiconductor laser (laser diode - LD) or a light-emitting diode (LED), used in optical communication and other applications.

10 2. Description of the Related Art

Generally, in an apparatus, such as an optical transmission apparatus, that uses a light-emitting device, the light output of the device must be controlled to a specified value. On the other hand, the light-producing efficiency of a light-emitting device such as an LD has a strong temperature dependence, and furthermore, the efficiency changes with age. Accordingly, to control the light output to a constant value under all possible conditions, the current supplied to the light-emitting device must be controlled to a proper value. Traditionally, negative feedback control is used to control the light output of a light-emitting device to a constant value. Figure 1 shows a prior art light output control circuit for controlling the light output of a light-emitting device. The operation of this circuit will be described below.

A drive current modulated with data in an LD driving circuit 10 is supplied to a light-emitting device 12. The peak value of this drive current (hereinafter called the drive current value) is controlled in proportion to a digital value input to a D/A conversion circuit 14. The digital value is supplied from a counter 16 placed directly before it. That is, the drive current value obtained is proportional to the counter value.

A photodiode (PD) 18 produces a monitor current proportional to the amount of light emitted by the light-

emitting device (LD), and a monitor section 20 converts the monitor current value into a voltage value and holds its peak value. The output of the monitor section 20 is compared with a reference value (voltage) 24 using a comparator 22, and the count value of the counter 16 is manipulated in accordance with the result of the comparison. That is, if the monitor output is smaller than the reference value, the counter value is incremented by 1 to increase the drive current value; on the other hand, if the monitor output is larger than the reference value, the counter value is decremented by 1 to decrease the drive current value. With this operation, the light output is controlled at a constant value with respect to the reference value, using negative feedback control.

At this time, the drive current value is controlled with an accuracy equivalent to the resolution determined by the least significant bit (LSB) of the D/A conversion circuit 14. For example, when a 10-bit D/A conversion circuit is used, a resolution of $2^{10}=1024$ is obtained. When controlling the output current within a range of 10 to 100 mA using this circuit, a current mirror circuit in the LD driving circuit 10 is designed so that 1 LSB corresponds to 0.1 mA, with digital values 100 to 1000 corresponding to drive current values 10 to 100 mA. In this case, since, at the minimum value 10 mA of the drive current, the current 0.1 mA per LSB corresponds to 1%, the above circuit can control the drive current with an accuracy of about 1% (the light output is also proportional to it). The prior art has achieved highly precise control using the above-described circuit.

The problem of the prior art output control circuit is that it takes time for the light output to reach the desired value, that is, the rise time is long.

Figure 2 shows the operating characteristic of the prior art light output control circuit. Time is

plotted along the abscissa and the drive current value along the ordinate. The value of the counter circuit is reset at power on. When the above-described feedback is activated, the counter value is updated by incrementing or decrementing by 1 at a time, depending on the result of the comparison made between the output of the monitor section 20 and the reference value 24, and the drive current value is updated accordingly, causing the drive current to change in a steplike manner. At this time, the drive current value changes in steps of 0.1 mA which is proportional to the current corresponding to the least significant bit (LSB) of the D/A conversion circuit. When the drive current value reaches the target value, the drive current value oscillates between two values, one above and the other below the target value, and a light output value stabilized within this range is obtained.

In this prior art, since the digital value is incremented or decremented in steps of 1 after power on until reaching the target value, if the difference between the target value and the current value (digital value) at power on is large, it takes a large number of steps until the current rises to the desired value, and the rise time thus becomes long.

In access optical communication systems that have recently entered commercial service, a burst transmission method that divides data into cells and transmits them in bursty manner has to be employed as the method of transmission between the subscriber and the network. Figure 3 shows the operation when the prior art light output control circuit is applied for burst transmission applications, to explain the problem of the prior art. As in Figure 2, the time is plotted along the abscissa and the drive current value along the ordinate.

When starting up a burst transmission apparatus, only a short period of time of a few microseconds allocated to initial starting cells is

allowed for the light output to rise to the target value. Accordingly, if the prior art light output control circuit were used for burst transmission, the light output could not rise fully during the starting cell period and hence could not be stabilized before the output of ordinary communication cells. Consequently, the prior art light output control circuit cannot be used for such applications.

For example, when the counter is started at an initial value 0 and is operated to count up until a maximum drive current value of 100 mA is obtained using, for example, a 10-bit D/A conversion circuit, in the worst case the counter would have to be updated 1024 times before the output is stabilized.

Thus the prior art has had the problem that it cannot be used for burst transmission applications because the rise time is long.

In the case of continuous transmission also, data cannot be transmitted during the start-up period. If the rise time of the optical module transmitter is long, the problem is that it takes time to start up the entire system. This also limits the time margin of the system or slows the system power up.

Another problem that arises when the prior art of Figure 1 is used for burst transmission concerns the control when no cells exist. In the prior art of Figure 1, since the control of the counter 16 is performed at all times regardless of the presence or absence of a signal, the time constant of the monitor section 20 must be made sufficiently long in order to maintain stable control even when there are no cells. Increasing the time constant, however, leads to the problem of slow response.

A further problem with the prior art of Figure 1 concerns very small fluctuations occurring after the control has reached a steady-state condition. As shown in Figure 2, in the prior art light output control

circuit, after the start up of the light output control circuit is completed and steady state is reached, the light output value continually oscillates between two values around the reference value. Usually, the circuit is designed to control the light output within specified limits despite the variations between the two values, but the light output value cycles through unnecessary changes.

Especially, in burst transmission, the time required for the light output to stabilize must be shortened; to achieve this, the feedback loop speed must be increased, but if the feedback is always performed at high speed, unnecessary updates will be repeated. This problem will result in increased error rate at the optical signal receiving end.

Furthermore, in the prior art light output control circuit, when the light output control circuit updates its light output value, the digital code input to the D/A conversion circuit 14 changes, and at this time, a spike called a glitch occurs. This glitch appears in the drive current, causing waveform distortion. This problem also results in increased error rate at the optical signal receiving end.

SUMMARY OF THE INVENTION

Accordingly, it is a first object of the present invention to provide a light output control circuit that rises quickly when starting.

It is a second object of the present invention to provide a light output control circuit that is suitable for burst transmission.

It is a third object of the present invention to provide a light output control circuit that can reduce the fluctuations after the light output is stabilized.

It is a fourth object of the present invention to provide a light output control circuit that is less prone to glitches caused by D/A conversion.

The first object is achieved by providing a light

output control circuit comprising: a photodetector which detects the light output of a light-emitting device; a comparator which compares a light output detection value with a reference value; a light output control device which controls the light output of the light-emitting device in a discrete manner in accordance with the result of the comparison output from the comparator; and a switching circuit which counts the number of control actions performed by the light output control device, and which instructs the light output control device to perform control in accordance with a start-up mode until the number of control actions after starting the control reaches a predetermined value, and to perform control in accordance with a steady-state mode after the number of control actions has reached the predetermined value.

The first object is also achieved by providing a light output control circuit comprising: a photodetector which detects the light output of a light-emitting device; a comparator which compares a light output detection value with a reference value; a light output control device which controls the light output of the light-emitting device in a discrete manner in accordance with the result of the comparison output from the comparator; and a switching circuit which instructs the light output control device to perform control in accordance with a start-up mode until the light output detection value, after the start of the control, enters a window of a prescribed width, and to perform control in accordance with a steady-state mode after the detection value has entered the window.

The first object is also achieved by providing a light output control circuit comprising: a photodetector which detects the light output of a light-emitting device; a comparator which compares a light output detection value with a reference value; a light output control device which controls the light output of the light-emitting device in a discrete manner in accordance

with the result of the comparison output from the comparator; and a switching circuit which instructs the light output control device to perform control in accordance with a start-up mode until the control history of the light output control device, after starting the control, matches a prescribed pattern, and to perform control in accordance with a steady-state mode after the control history has matched the prescribed pattern.

The second object is achieved by providing a light output control circuit comprising: a photodetector which detects the light output of a light-emitting device; a comparator which compares a light output detection value with a reference value; a light output control device which controls the light output of the light-emitting device in a discrete manner in accordance with the result of the comparison output from the comparator; and a clock control circuit which detects data to be supplied to the light-emitting device, generates a clock in accordance with the result of the detection, and supplies the clock as a timing signal indicating control timing to the light output control device.

The third object is achieved by providing a light output control circuit comprising: a photodetector which detects the light output of a light-emitting device; a comparator which compares a light output detection value with a reference value; a light output control device which controls the light output of the light-emitting device in a discrete manner in accordance with the result of the comparison output from the comparator; and an update permit control circuit which, after the light output has stabilized, prohibits updating of a control value for the light output from the time that the control value is last updated, until the time that a prescribed condition is satisfied.

The fourth object is achieved by providing a light output control circuit comprising: a photodetector which detects the light output of a light-emitting device; a

comparator which compares a light output detection value with a reference value; and a light output control device which controls the light output of the light-emitting device in a discrete manner in accordance with the result of the comparison output from the comparator, wherein, after the light output has stabilized, the frequency band of a drive current for the light-emitting device is reduced in width.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of a prior art light output control circuit;

Figure 2 is a graph for explaining the operation of the circuit of Figure 1;

Figure 3 is a diagram showing a burst signal;

Figure 4 is a block diagram of a first embodiment of the present invention;

Figure 5 is a timing chart for explaining the operation of the circuit of Figure 4;

Figure 6 is a circuit diagram showing one example of a counter 16;

Figure 7 is a circuit diagram showing one example of a coarse/fine switching circuit 26;

Figure 8 is a timing chart for explaining the operation of the circuit of Figure 7;

Figure 9 is a circuit diagram showing one example of a clock control circuit 28;

Figure 10 is a timing chart for explaining the operation of the circuit of Figure 9;

Figure 11 is a circuit diagram showing one example of an LD driving circuit 10;

Figure 12 is a block diagram of a second embodiment of the present invention;

Figure 13 is a circuit diagram showing one example of a monitor section 20;

Figure 14 is a timing chart showing the operation of the second embodiment;

Figure 15 is a diagram showing the operation of a

third embodiment;

Figure 16 is a block diagram of the third embodiment;

5 Figure 17 is a circuit diagram showing one example of the counter 16 used in the second embodiment;

Figure 18 is a circuit diagram showing one example of a coarse/fine switching circuit 76;

Figure 19 is a timing chart showing the operation of the circuit of Figure 18;

10 Figure 20 is a diagram showing the operation of a fourth embodiment of the present invention;

Figure 21 is a graph for explaining the operation of the fourth embodiment;

15 Figure 22 is a block diagram of the fourth embodiment;

Figure 23 is a circuit diagram showing one example of the counter 16 used in the fourth embodiment;

Figure 24 is a timing chart showing the operation of the fourth embodiment;

20 Figure 25 is a circuit diagram of a coarse/fine switching circuit 82;

Figure 26 is a diagram showing the operation of a fifth embodiment of the present invention;

25 Figure 27 is a block diagram of the fifth embodiment;

Figure 28 is a circuit diagram of a coarse/fine switching circuit 88;

Figure 29 is a circuit diagram showing one example of level shift voltage sources 98 and 100;

30 Figure 30 is a graph showing the current versus light output characteristics of a laser diode;

Figure 31 is a block diagram of a sixth embodiment of the present invention;

35 Figure 32 is a diagram showing the operation of a seventh embodiment of the present invention;

Figure 33 is a block diagram of the seventh embodiment;

Figure 34 is a circuit diagram showing one example of a coarse/fine switching circuit 108;

Figure 35 is a circuit diagram showing another example of the coarse/fine switching circuit 108;

5 Figure 36 is a block diagram of an eighth embodiment of the present invention;

Figure 37 is a circuit diagram showing one example of a coarse/fine switching circuit 116;

10 Figure 38 is a block diagram of a ninth embodiment of the present invention;

Figure 39 is a circuit diagram showing one example of a coarse/fine switching circuit according to a 10th embodiment of the present invention;

15 Figure 40 is a block diagram of an 11th embodiment of the present invention;

Figure 41 is a circuit diagram showing one example of a coarse/fine switching circuit 124;

Figure 42 is a block diagram of a 12th embodiment of the present invention;

20 Figure 43 is a circuit diagram showing one example of a coarse/fine switching circuit 126;

Figure 44 is a block diagram of a 13th embodiment of the present invention;

25 Figure 45 is a circuit diagram showing one example of a coarse/fine switching circuit 128;

Figure 46 is a circuit diagram showing one example of a coarse/fine switching circuit 230 according to a 14th embodiment of the present invention;

30 Figure 47 is a circuit diagram showing one example of a clock control circuit 72;

Figure 48 is a timing chart showing the operation of the circuit of Figure 47;

Figure 49 is a circuit diagram showing one example of a data detection circuit 232;

35 Figure 50 is a circuit diagram showing one example of a monitor section 243;

Figure 51 is a circuit diagram showing another

example of the counter 16;

Figure 52 is a circuit diagram showing a second example of the clock control circuit 72;

5 Figure 53 is a timing chart showing the operation of the circuit of Figure 52;

Figure 54 is a circuit diagram showing another example of the clock control circuit 72;

Figure 55 is a circuit diagram showing one example of a data detection circuit 250;

10 Figure 56 is a circuit diagram showing still another example of the clock control circuit 72;

Figure 57 is a circuit diagram showing a further example of the clock control circuit;

15 Figure 58 is a circuit diagram showing one example of a data detection circuit 256;

Figure 59 is a timing chart showing signals at points A to J in Figure 57;

Figure 60 is a block diagram of another embodiment of the present invention;

20 Figure 61 is a circuit diagram of the LD driving circuit 10 in the embodiment of Figure 60;

Figure 62 is a circuit diagram of the counter 16 in the embodiment of Figure 60;

25 Figure 63 is a diagram showing a steady-state control condition;

Figure 64 is a diagram showing a D/A conversion glitch;

Figure 65 is a block diagram of still another embodiment of the present invention;

30 Figure 66 is a timing chart showing the operation of the embodiment of Figure 65;

Figure 67 is a timing chart showing the operation of still another embodiment of the present invention;

Figure 68 is a block diagram of the same embodiment;

35 Figure 69 is a block diagram of still another embodiment of the present invention;

Figure 70 is a circuit diagram showing one example

of an update permit control circuit 276;

Figure 71 is a circuit diagram showing one example of the LD driving circuit;

Figure 72 is a circuit diagram showing another
5 example of the LD driving circuit;

Figure 73 is a circuit diagram showing one example of a band switching circuit;

Figure 74 is a timing chart showing the operation of the circuit of Figure 73;

10 Figure 75 is a circuit diagram showing another example of the band switching circuit;

Figure 76 is a circuit diagram showing still another example of the band switching circuit;

15 Figure 77 is a block diagram of still another embodiment of the present invention;

Figure 78 is a block diagram of still another embodiment of the present invention;

Figure 79 is a block diagram of still another embodiment of the present invention;

20 Figure 80 is a block diagram of still another embodiment of the present invention;

Figure 81 is a block diagram of still another embodiment of the present invention;

25 Figure 82 is a block diagram of still another embodiment of the present invention;

Figure 83 is a block diagram of still another embodiment of the present invention;

30 Figure 84 is a circuit diagram showing another example of a coarse/fine switching and operation mode switching circuit;

Figure 85 is a timing chart showing the operation of the circuit of Figure 84;

Figure 86 is a circuit diagram showing another example of the update permit control circuit 276;

35 Figure 87 is a circuit diagram showing still another example of the update permit control circuit 276;

Figure 88 is a timing chart showing the operation of

the circuit of Figure 87;

Figure 89 is a circuit diagram showing a further example of the update permit control circuit 276;

5 Figure 90 is a timing chart showing the operation of the circuit of Figure 89;

Figure 91 is a circuit diagram showing a still further example of the update permit control circuit 276; and

10 Figure 92 is a timing chart showing the operation of the circuit of Figure 91.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 4 shows a first embodiment of the present invention. The same constituent elements as those in Figure 1 are designated by the same reference numerals.
15 In this embodiment, after resetting a coarse/fine switching circuit 26 by a reset signal, the counter 16 that controls the light output value is caused to count up or down with a large step a predetermined number of times, and then the operation mode of the counter 16 is
20 switched to count up or down in the small step. The present embodiment concerns a light output control circuit for use with a laser driving circuit for continuous transmission applications.

In the illustrated circuit, as in the prior art
25 circuit of Figure 1, a drive current modulated with a data signal in the LD driving circuit 10 is supplied to the light-emitting device. The drive current value is controlled using the counter 16 and the D/A conversion circuit 14. The monitor current proportional to the LD
30 output is I/V converted by the monitor section 20, and the result is compared with the reference value 24 to manipulate the counter 16. If a 10-bit D/A converter is used as the D/A conversion circuit 14, and a drive
current of 0.1 mA is made to correspond to a digital
35 value 1, the controllable range of the drive current is 0 to 102.3 mA.

A conventional voltage regulation circuit using a

BRG or a Zener diode is used to provide the reference value. A differential amplifier circuit is used as the comparator 22. Since this control circuit is used for continuous transmission, the monitor section 20 uses an
5 average value detection circuit comprising a resistor and a capacitor. It is also possible to create the reference value by inputting a data signal to a circuit similar to the monitor section.

The present embodiment differs from the prior art of
10 Figure 1 by the inclusion of a mechanism for switching the counter 16 between coarse and fine settings to control the drive current. In the present embodiment, the coarse/fine switching is performed based on the number of feedback operations (the number of updates of
15 the up/down counter) during initial power up.

The coarse/fine operation of the counter 16 is controlled by a coarse/fine switching signal which is output from the coarse/fine switching circuit 26. The coarse/fine switching circuit 26 is controlled by a clock
20 and the reset signal 27. The clock supplied to the counter 16, coarse/fine switching circuit 26, and D/A conversion circuit 14 is created by a clock control circuit 28.

The operation of the present embodiment will be
25 described below with reference to Figure 5.

Initial start up 30: The value of the counter 16 and the value of a counter in the coarse/fine switching circuit 26 are cleared by an initial start-up reset signal (low). At this time, the coarse/fine switching
30 output is high to indicate coarse operation mode.

Coarse operation mode 32: When the clock and data are input, the LD driving circuit 10 outputs a drive current modulated with the data. First, the current value is 0 mA because the counter 16 is reset. Next, the
35 monitor current value is compared with the reference value, as a result of which the value of the counter 16 increases. Since the coarse/fine switching signal is

high (indicating coarse operation), the counter value increases by 32 each time the counter 16 is updated, and the drive current thus rises by 3.2 mA each time. This operation is repeated until the drive current reaches the target value and, once the target value is reached, the current value oscillates around the target value, varying between two values with a difference of 3.2 mA. The number of updates of the counter 16 up to this point is reduced to $1/M$ (in the illustrated example, $1/32$), and the rise time can be shortened correspondingly. In the illustrated example, when the counter 16 is operated starting at its initial value 0, the maximum current value of 102.4 mA can be reached with 32 updates in the worst case.

The clock supplied to the counter 16 and coarse/fine switching circuit 26 is a slow clock derived by frequency-dividing the base clock by 128, considering the time constant of the average value circuit in the monitor section 20. The frequency-divided clock is generated within the clock control circuit 28 (described in detail later).

The coarse operation mode ends when the counter (described in detail later) in the coarse/fine switching circuit 26 has counted up to 32; thereupon, the output of the coarse/fine switching circuit 26 changes to low, stopping the counter, while causing the mode to switch to the fine operation mode. The update cycle of the counter 16 is equal to the cycle of the frequency-divided clock, and the duration of the coarse operation mode in this embodiment is $128 \times 32 = 4096$ times the cycle of the base clock.

Fine operation mode 34: In the fine operation mode, the counter 16 updates its value in increments of a minimum unit 1. Consequently, the drive current changes in increments of 0.1 mA, approaching the final steady-state value. Once the target value is reached, the drive current value oscillates between two values closest to

the target value. The number of updates of the counter 16 required to reach the final steady-state value after entering the fine operation mode is M or less (in the illustrated example, 32 or less). Accordingly, the steady-state value can be reached with $32 + 32 = 64$ updates (coarse and fine operation modes combined) under worst case conditions. In the prior art, it takes 1024 updates in the worst case. In the present embodiment, therefore, the speed is increased by a factor of more than 10.

Figure 6 shows a detail circuit block diagram of the counter 16. This circuit comprises a 10-bit up/down counter which stores a drive current control value and is capable of switching between coarse and fine modes. The 10-bit up/down counter is implemented by connecting two 5-bit up/down counters 36 and 38. The meanings of input/output signals of the 5-bit up/down counters 36 and 38 are given below.

UP: Up/down input. High for UP and low for DOWN.
CL: Clear input. Low for clear.
CK: Clock input.
EN: Enable input. High to operate and low to hold.
CO: Carry output. High when carry or borrow occurs.
D0 - D4: LOAD data inputs.
L0 - L4: LOAD control input. High to load LOAD data in the corresponding bit.
O0 - O4: Output (count value) data.

The operation of the circuit of Figure 6 constructed by connecting the two 5-bit counters will be described below.

(1) When coarse/fine switching signal = H (Coarse operation mode)

When the coarse/fine switching signal is high, since all the LOAD inputs of the up/down counter 36 are high, the output of the comparator is loaded into all the bits of the count value of the up/down counter 36. The output of the comparator is also input to the up/down input of

the counter 36. When the monitor value is smaller than the reference value, and therefore the output of the comparator is high, all the bits of the counter 36 are 1s. Since, at this time, the up/down input is high (UP), a carry occurs for every clock. If the output of the comparator is low, all the bits of the counter 36 are 0s, and the up/down input is low (DOWN), so that a borrow occurs for every clock. When a carry or a borrow occurs in the counter 36, the up/down counter 38 is enabled via an AND gate 37. Since the L0 to L4 inputs of the high-order counter 38 are low, data is not loaded and the high-order counter 38 counts up or down. That is, D0 to D4 of the high-order counter 38 count up or down in accordance with the up/down signal supplied from the comparator 22.

In this way, in the coarse operation mode, all 1s or all 0s are loaded into the low-order five bits by the up or down signal, and the resulting carry or borrow causes the high-order 5-bit counter 38 to count up or down, thus accomplishing the coarse mode operation.
(2) When coarse/fine switching signal = L (Fine operation mode)

Since the L0 to L4 inputs of both the high-order and low-order counters are all low, the counters together operate as a normal 10-bit up/down counter with all 10 bits (5×2) counting up or down (fine mode operation).

In this way, the counter 16 operates as an up/down counter whose operation mode is switchable between the coarse operation and fine operation modes by the coarse/fine switching signal.

Figure 7 shows a detailed circuit block diagram of the coarse/fine switching circuit 26, and Figure 8 shows the circuit operation. This circuit generates the coarse/fine switching signal from the reset signal and clock signal. The circuit comprises a 5-bit binary counter 40 and an inverter 42.

At initial start up, the reset signal is low to

reset the contents of the counter. When the clock is input, the counter counts up, and when the counter counts up to $32 = 2^5$, the carry output CO goes high, which is inverted by the inverter 42 and applied as a low signal to the enable terminal E to stop the counter operation. Accordingly, after the reset state is released, the coarse/fine switching output is held high until 32 clock pulses are counted, and thereafter goes low. Since this clock is the same clock supplied to the light output control counter 16, the counter 40 counts the number of updates of the counter 16. The coarse/fine switching function is accomplished by counting the predetermined number of times that the counter 16 is updated in the coarse operation mode.

In Figure 7, the present embodiment uses a counter of the type that counts up to 32, but if another count number is to be used, a counter of the appropriate type should be used.

Figure 9 shows a detailed circuit block diagram of the clock control circuit 28, and Figure 10 shows the circuit operation. This clock control circuit is designed for continuous transmission. The base clock is frequency-divided by a factor of 128 to create the counter clock which is supplied to the counter 16 as well as to the coarse/fine switching circuit 26. The frequency dividing circuit consists of seven D-FF (flip-flop) circuits 44, and produces one output clock cycle for every 128 input clock cycles. The clock to be supplied to the D/A conversion circuit 14 is delayed by half a cycle by a D-FF 46.

Figure 11 shows a detailed circuit diagram of the LD driving circuit 10. This circuit, using differential data signals output from inverters 48 and 50 and a differential pair consisting of n-channel MOS transistors 52 and 54, modulates the current delivered from an n-channel MOS transistor 56 acting as a current source, and produces the drive current (modulated current) to be

supplied to the LD.

5 The current value of the constant current source 56 is provided by an output current of a current mirror consisting of the n-channel MOS transistors 56 and 58, and its input current is obtained from a current mirror consisting of p-channel MOS transistors 60 and 62, whose input current in turn is obtained by converting the D/A converter output voltage into a constant current value using an operational amplifier 64, an n-channel MOS transistor 66, and a fixed resistor 68. Accordingly, the 10 drive current value is controlled by the output of the D/A conversion circuit 14. The above description has assumed that the output of the D/A conversion circuit is a voltage signal, but if the output is a current, the output can be coupled directly to the current mirror circuit consisting of the transistors 60 and 62 or to the current mirror circuit consisting of the transistors 56 and 58. 15

20 As described, in the first embodiment, after resetting the coarse/fine switching circuit, the counter value that determines the light output is increased or decreased in incremental steps a predetermined number of times, the step size being M times the value indicated by the least significant bit of the counter, and after that, 25 the value indicated by the least significant bit of the counter is counted up or down. This speeds the power up of the light output control circuit which is designed for use with the laser diode driving circuit for continuous transmission applications.

30 In the present embodiment, an external signal is used as the reset signal, but instead, use can also be made of a signal that a supply voltage detection circuit (such as a conventional power-on reset circuit) or the like automatically generates when a supply voltage is 35 turned on.

To quickly raise the light output to or near the target value, the step size in the coarse operation

should be increased, but increasing the coarse operation step size will result in increasing the number of steps required to reach the final steady-state value after entering the fine operation mode. Assuming that the
5 number of bits of the D/A conversion circuit is N, and that the coarse operation step size is equal to the Mth lowest bit, then $2^{(N-M)}$ coarse operation steps and 2^M fine operation steps, a total of $2^{(N-M)} + 2^M$ steps, are required to scan the full range of digital values of the D/A
10 conversion. The total number of steps is the smallest when $M = N/2$.

That is, when a 10-bit D/A converter is used, it is best to set the number of coarse operation steps to 32, in which case all digits settle down after 64 steps.

15 In the above embodiment, the number of coarse operation steps is set to 32 ($32 \times 32 = 1024$) to scan all the digital values 0 to 1023 input to the 10-bit D/A conversion circuit, but when there is no need to scan the full range during power up, for example, when loading an
20 initial value into the counter, or when the electric current range used is narrow, it is desirable to reduce the number of counts because the rise time can then be shortened.

In the present embodiment, at reset, the value of
25 the light output control counter 16 is reset, but this does not necessarily requires loading the value 0 into the counter 16. For some reason, an initial value may be loaded. For example, when a value corresponding to a current larger than the target value is used as the
30 initial value, it is possible to set the counter 16 to start counting from that value, decrementing by 16 for each update. Furthermore, an appropriate initial value may be loaded in accordance with the type of LD, the value of the current supplied, or the light output
35 accuracy required.

If a value appropriate to the temperature at that time and the temperature characteristic of the LD is

loaded as the initial value of the light output control, the desired light output can be obtained starting from the first bit of the first burst signal, and thus, fast response and high precision control of the light output can be achieved at the same time. Furthermore, by performing the above-described initialization between bursts, the light output can be adjusted to compensate for abrupt changes in ambient temperature between burst signals.

10 In the present embodiment, the 10-bit up/down counter has been described as being constructed by connecting two 5-bit counters; alternatively, two 4-bit counters and one 2-bit counter may be connected together or a 10-bit counter as a single unit may be used.

15 Figure 12 shows a second embodiment. This embodiment is applicable for both burst transmission and continuous transmission, and differs from the first embodiment (Figure 4) in the configuration of the monitor section and clock control circuit.

20 Figure 13 shows a circuit diagram of the monitor section 70. This circuit comprises an I/V conversion circuit 73 and a peak-hold circuit 74. While the monitor section of the first embodiment can be applied only to continuous transmission because of the use of the average value detection circuit having a long time constant, the present embodiment can be applied to burst transmission as well as to continuous transmission because the monitor value of the light output can be detected instantaneously by capturing the peak value of the light output.

25 Spontaneous discharge through a resistor 75 is used to discharge a current and follow the change when an update is made in a direction that reduces the light output value. The peak-hold circuit used in the present embodiment may be replaced by a bottom-hold circuit or a sample-and-hold circuit.

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In the clock control circuit 28 of the first embodiment, the clock supplied to the counter was derived

by simply dividing the base clock to accommodate continuous transmission. In burst transmission, on the other hand, time intervals during which no data are transmitted are relatively long, and during these intervals, the light output value cannot be fed back. In view of this, the clock control circuit 72 of the second embodiment is configured to stop the supply of the clock to the counter 16, coarse/fine switching circuit 26, and D/A conversion circuit 14 during no-data periods so as not to update the control condition when there are no data.

Figure 14 shows the operation of the present embodiment. The difference from the first embodiment is that during no-data periods, the clock supplied to the counter 16 is stopped to prevent the counter 16 from being updated. The detailed configuration of the clock control circuit 72 will be described later.

In the first and second embodiments, a quick rise is achieved by switching between the coarse operation and fine operation modes, but by increasing the number of steps in the coarse operation mode, the rise time before the final bit stabilizes can be further shortened (multi-stage counting method).

Figure 15 shows the operation of a third embodiment for implementing the above operation.

During the initial power up of the light output control counter, first the counter is updated 32 times by counting up or down the sixth bit of the counter in increments of 32 LSBs, thus increasing or decreasing the drive current in steps of 3.2 mA. Next, the counter is updated four times by counting up or down the fourth lowest bit of the counter in increments of 8 LSBs, thus increasing or decreasing the drive current in steps of 0.8 mA. Thereafter, the counter is updated in increments of 1 LSB, thus increasing or decreasing the drive current in steps of 0.1 mA. In this embodiment, the counter is updated $32 + 4 + 8 = 44$ times until the final bit of the

counter stabilizes, reaching a steady-state value. This provides an improvement in speed by a factor of 1.5 compared with the second embodiment that required $32 + 32 = 64$ updates.

5 Figure 16 shows the circuit block configuration for implementing the third embodiment. The major difference from the second embodiment is that the coarse/fine switching circuit 76 outputs two coarse/fine switching signals for supply to the light output control counter 16 to realize two coarse operation modes.

10 Figure 17 shows a circuit diagram of the light output control counter 16 used in the above configuration. The difference from the counter of Figure 6 used in the first and second embodiments lies in the connections associated with the two coarse/fine switching signals. That is, the coarse/fine switching signals 1 and 2 are coupled to their associated bits at the LOAD control inputs of the low-order counter. While the corresponding switching signal is held high, a high state is loaded into each associated bit when counting up or a low state when counting down. The low-order bits 4 and 5 (positions 8 and 16) of the low-order 5-bit counter are controlled by the coarse/fine switching signal 1. The low-order bits 1 to 3 (positions 1, 2, and 4) of the low-order 5-bit counter are controlled by the coarse/fine switching signal 2.

25 Figure 18 shows a circuit diagram of the coarse/fine switching circuit for generating the coarse/fine switching signals 1 and 2, and Figure 19 shows the circuit operation. This circuit, unlike the circuit shown in Figure 7, comprises two counter circuits.

30 After the reset signal is released (low to high), a clock signal is supplied to operate a 5-bit counter 78, and when the counter has counted up to 32, the counter 78 is stopped, at which point the coarse/fine switching signal 1 changes from high to low. With the carry output of the counter 78 going high, the CL terminal of a

35

counter 80 goes high, causing the 2-bit counter 80 to start counting. When the counter 80 has counted up to 4, the counter 80 is stopped, and the coarse/fine switching signal 2 changes from high to low.

5 In the third embodiment, two coarse operation modes are provided to improve rise speed. To further improve the speed, it will be effective to increase the number of coarse operation modes. This can be accomplished by increasing the number of coarse/fine switching signals
10 and providing control circuits for controlling them.

 If the number of coarse operation mode stages is further increased to provide a coarse operation mode for each bit, the fastest rise speed can be achieved. Figure 20 shows the operation of a fourth embodiment (bisection
15 method) according to the present invention.

 After resetting, the light output control counter is updated 32 times by counting up or down the sixth and higher bits of the counter in increments of 32 LSBs, thus increasing or decreasing the drive current in steps of
20 3.2 mA, as in the second embodiment. The characteristic feature of the fourth embodiment is that the updating bit is lowered by one for each of the subsequent updates. That is, the counter is updated once by counting up or down the fifth and higher bits (second coarse operation
25 mode), then the lowest bit is sequentially lowered for each subsequent update, such as the fourth and higher bits (third coarse operation mode), the third and higher bits (fourth coarse operation mode), the second and higher bits (fifth coarse operation mode), and so on,
30 until finally determining the least significant bit (LSB), reaching a final steady-state value. In this embodiment, the counter is updated $32 + 5 = 37$ times before the final bit of the counter stabilizes, reaching a steady-state value. This achieves a faster speed
35 compared with the second embodiment that required 44 updates.

 A theory of how the rise speed can be improved

according to the fourth embodiment will be described below. The power up process of the light output control circuit corresponds to finding a variable X for which the light output $F(X)$, a function of X , equals the target value V . This means determining $X = F^{-1}(V)$ for which $F(X) = V$. Figure 21 shows the graph of $X-F(X)$. For example, when the function is known to monotonically increase or decrease over an interval $X = 0$ to 32 , that is, $F(0) < V < F(32)$, then $X = F^{-1}(V)$ exists within the interval of 0 to 32 .

One method of obtaining the X is the bisection method. The bisection method is an iterative method for finding a solution; that is, when a solution is known to exist within a certain interval, the midpoint of the interval is obtained and the interval containing the solution is narrowed to one half the length of the original interval, and this process is repeated. If the variable X is a binary number (digital), this method corresponds to successively determining bits in the digital value, starting from the highest-order bit, and the solution can be found by repeating the process the same number of times as the number of bits in the digital value. In the fourth embodiment, during initial power-up the counter is caused to count up or down the sixth and higher bits to obtain an interval containing the solution, and then the bisection method is applied to the low-order five bits. With this bisection method, the solution can be found by five iterations.

Figure 22 shows the circuit block configuration for implementing the fourth embodiment. The difference from the second embodiment is that there are five coarse/fine switching signals.

Figure 23 shows a circuit diagram of the light output control counter 16 used in the above configuration. The difference from the counter of the second embodiment shown in Figure 6 lies in the connections associated with the coarse/fine switching

signals. That is, the five coarse/fine switching signals are coupled one for one to their associated bits at the LOAD control inputs L0 to L4 of the low-order counter. By applying the waveforms of Figure 24 as the coarse/fine switching signals, the sixth and higher bits of the counter can be counted up or down 32 times in the coarse mode, and then the fifth to the least significant bits can be successively determined using the bisection method, as described above.

Figure 25 shows a circuit diagram of the coarse/fine switching circuit for generating the coarse/fine switching signals. This circuit, unlike the circuit shown in Figure 18, comprises a 5-bit counter 84 for counting up to 32 and four 1-bit counters 80 each for counting 1.

In the above fourth embodiment, during initial power-up, the counter is caused to count up or down the sixth and higher bits to obtain an interval containing the solution, and after that, the bisection method is applied; alternatively, the bisection method may be applied from the beginning, starting with the counting up or down of the highest-order 10th digit (or higher) at initial power on. In this case, with a 10-digit or 10-bit binary counter, if the value is updated for each digit starting from the highest-order digit, the target value can be reached with 10 updates.

In the above fourth embodiment, the coarse operation using the bisection method is accomplished by counting up or down once for each bit, but the number of counts for each bit need not necessarily be limited to 1. Though the illustrated example achieves the fastest speed, the number of counts for each bit may be increased for some other reason.

Figure 26 shows the operation of a fifth embodiment according to the present invention. In this embodiment, the coarse/fine switching is effected by detecting the light output nearing the target value. In the first to

fourth embodiments described above, the timing of the coarse/fine switching has been determined so that the coarse mode operation is performed a predetermined number of times during initial power up; by contrast, in the present embodiment, the coarse/fine switching is performed by determining whether the light output is nearing stabilization. This determination is made by providing a window of a predetermined width near the target value and by detecting whether the monitor value has entered this window.

Figure 27 shows a block diagram of this embodiment. The difference from the first to fourth embodiments is that the coarse/fine switching circuit 88 is supplied with the monitor value and reference value signals.

Figure 28 shows the configuration of the coarse/fine switching circuit 88. The coarse/fine switching circuit 88 comprises a window comparator 90 and a latch 92. The window comparator 90 includes two comparators 94 and 96, each constructed from a differential amplifier circuit, that compare the monitor output with the respective reference values created by shifting the input reference value by voltages $\Delta Vw1$ and $\Delta Vw2$ supplied from level shift voltage sources 98 and 100. The comparison results are then NORed, and the result of the NORing is output as the window comparator output. That is, when the monitor value enters the window of the width $\Delta Vw1 + \Delta Vw2$, the window comparator output goes high.

The latch 92 is provided to implement the coarse operation mode after resetting. A JK flip-flop 102 is used as the latch. At power up, the latch 92 is reset, and latch $XQ = \text{High}$ is output as the output of the coarse/fine switching circuit, thereby sending a coarse operation mode signal. When the coarse mode power up proceeds to the point where the monitor value enters the window, latch J input goes high, causing the XQ output to go low and thus sending a fine operation mode signal.

Here, the window width must be made larger than the width of change of the monitor value per control action in the coarse operation mode. When the window width is smaller, if the monitor value goes up or down exceeding the range of the window in the coarse operation mode, the coarse operation mode might continue infinitely.

Figure 29 shows a further detailed circuit diagram of the level shift voltage sources 98 and 100 in the window comparator. In the circuit shown, the level shift voltage sources are realized by passing currents $I_{w1} = I_{w2} = 50 \mu A$ through two resistors R_{W1} and R_{W2} , respectively. Component values are, for example, $R_{W1} = R_{W2} = 1 k\Omega$ and $I_{w1} = I_{w2} = 50 \mu A$, and as a result, $\Delta V_{w1} = \Delta V_{w2} = 50 mV$ is obtained. The current I_{w1} is produced by duplicating, through a current mirror consisting of p-channel MOS transistors M2 and M4, the output current of a constant current circuit comprising a reference voltage source (a conventional constant voltage circuit such as a Zener diode type or a BGR type), a resistor R1, an operational amplifier, and an n-channel MOS transistor M1. Likewise, the current I_{w2} is produced by transferring the output current of the constant current circuit through a current mirror consisting of p-channel MOS transistors M2 and M3, and by duplicating it through a current mirror consisting of n-channel MOS transistors M5 and M6.

As a modification of the fifth embodiment, if the window width of the window comparator is made temperature dependent, the rise time can be further shortened. The principle behind this idea will be explained with reference to Figure 30. Figure 30 shows the current versus light output characteristics of a laser diode. Lasing occurs when the drive current exceeds the threshold, but the differential efficiency $= \Delta I / \Delta I$ has a pronounced temperature dependence and decreases with increasing temperature. Accordingly, in digital control

of the drive current, the rate of change of light amount with respect to the digital value change of 1 decreases as the temperature increases. As a result, if the window width is fixed, the number of updates required until
5 stabilization is achieved after entering the fine operation mode will increase at high temperatures. To address this problem, at high temperatures the window width is reduced in proportion to the temperature dependence of the light amount step size (proportional to
10 the laser's differential efficiency), thereby eliminating the temperature dependence of the number of updates required until stabilization is achieved after entering the fine operation mode. This serves to shorten the rise time over a wide temperature range.

15 In a specific method for achieving this, the fixed resistor R1 in the constant current generating circuit of Figure 29 is replaced by a positive temperature coefficient resistor (also called a positive temperature coefficient thermistor) having temperature dependence, or
20 a resistor constructed by combining such a resistor with a fixed resistor, so that the voltage of the voltage source that determines the window width can be reduced with increasing temperature.

In the above description of the window comparator,
25 the level shift voltages are shown as being set $\Delta V_{w1} = \Delta V_{w2}$, but these voltages need not necessarily be set identical. Similarly, R_{W1} and R_{W2} need not necessarily be made equal to each other.

Figure 31 shows a sixth embodiment. This embodiment
30 is identical to the fifth embodiment, except that the coarse operation mode is divided into two stages. Two coarse/fine switching circuits are therefore provided. The counter 16 is the same as that used in the third embodiment shown in Figure 17. The coarse/fine switching
35 circuit 104, in which the window of the window comparator is the larger, outputs a coarse/fine switching signal 1,

and the coarse/fine switching circuit 106, in which the window of the window comparator is the smaller, outputs a coarse/fine switching signal 2.

5 With the above configuration, the sixth embodiment improves rise time by switching the operation of the up/down counter between the coarse and fine modes using the plurality of window comparators during initial power up.

10 Figure 32 shows the operation of a seventh embodiment. This embodiment uses an update history of the light output control counter to detect whether the light output is nearing the target value. More specifically, in the light output control circuit using the comparator and the light output control up/down
15 counter, the comparator output applied to update the up/down counter is such that when there is a disparity between the light output and the target value, only an UP control or DOWN control is repeated, and once the light output is stabilized, UP control and DOWN control are
20 repeated alternately. Accordingly, by keeping UP/DOWN history records, and checking whether UP control and DOWN control are mixed, it can be determined whether the light output has stabilized or not in the coarse operation mode.

25 Figure 33 shows the configuration of the seventh embodiment. The difference from the other embodiments is that the output of the comparator is also connected to the coarse/fine switching circuit 108.

30 One specific example of the coarse/fine switching circuit 108 is shown in Figure 34. This circuit stores the output history of the comparator in a shift register 110, and generates a signal based on the logic state of each digit. When the digits of the register differ from each other, i.e., the state "101" or "010", this state is
35 detected using NAND circuits, and an XQ output of a latch 112 is set low. With this configuration, the coarse/fine switching signal can be generated by detecting, based on

the comparator output history, that the light output has reached the target value in the coarse operation mode.

Another example of the coarse/fine switching circuit 108 is shown in Figure 35. This circuit stores the
5 output history of the comparator in a 5-bit shift register 114, and generates a signal based on the logic state of each digit. Whether the digits of the register differ from each other is detected using exclusive-OR (EXOR) circuits. The conditions for determining that the
10 target value is reached are expanded to include not only "010" and "010", but also "10010", "011010". "11010", "10101", "01010", and "00101".

Figure 36 shows an eighth embodiment of the present invention. This embodiment differs from the seventh
15 embodiment (Figures 32 and 33) by the provision of two coarse operation modes. In the circuit diagram, two coarse/fine switching signals are shown. A specific example of the coarse/fine switching circuit 116 is shown in Figure 37. This circuit differs from the circuit of
20 the seventh embodiment shown in Figure 34 in that two latches are provided to generate two coarse/fine switching signals to effect the two coarse operation modes.

Figure 38 shows a ninth embodiment of the present
25 invention. This embodiment includes a coarse/fine switching terminal so that the coarse/fine switching can be effected by the application of an external signal. In applications such as optical communication systems or the like, when the optical transmitter is constructed as a
30 module, various control signals are supplied from the main unit; this embodiment is particularly useful in applications where the coarse/fine switching signal is supplied from the main unit.

A 10th embodiment is a combination of the second
35 embodiment (counting method) and the fifth embodiment (window comparator). At power on, the sixth lowest bit of the counter 16 is caused to count up or down 32 times,

and then the fourth lowest bit of the counter 16 is caused to count up or down until the monitor value is brought inside the level width of the window comparator, and finally the lowest bit is caused to count up or down.

5 The entire configuration is the same as that shown in Figure 27, except that two coarse/fine switching signals are output. The configuration of the coarse/fine switching circuit is shown in Figure 39. First, a counter 18 performs counting and outputs the coarse/fine
10 switching signal 1. Next, a window comparator 120 performs coarse/fine control to accomplish the above-described operation.

Figure 40 shows an 11th embodiment. This embodiment is a combination of the second embodiment (counting
15 method) and the seventh embodiment (history recording, Figure 33). At start up, the sixth lowest bit of the counter is caused to count up or down; then, the third lowest bit of the counter is caused to count up or down until the output history of the comparator circuit shows
20 UP control and DOWN control in a mixed manner, and finally the lowest bit is caused to count up or down. The output of the comparator 22 as well as the clock necessary for counting is connected to the coarse/fine switching circuit 124.

25 One example of the coarse/fine switching circuit 124 is shown in Figure 41. First, a counter 122 (equivalent to the one shown in Figure 7) performs counting and outputs the coarse/fine switching signal 1. Next, a circuit (equivalent to the one shown in Figure 34)
30 performs coarse/fine control based on the output history of the comparator to accomplish the above-described operation.

Figure 42 shows a 12th embodiment. This embodiment is a combination of the fifth embodiment (window
35 comparator, Figure 27) and the fourth embodiment (bisection method, Figure 22). At power on, the sixth lowest bit of the counter is caused to count up or down

until the monitor value is brought inside the level width of the window comparator, then the fifth bit of the counter is caused to count up or down once, followed by counting up or down the fourth bit once; the process is
5 repeated to count up or down the value indicated by the bits higher than the least significant bit of the counter, and finally the least significant bit is counted up or down repeatedly to stabilize the light output.

In operation, the signal from the monitor section 70
10 and the reference value 24 are supplied to the coarse/fine switching circuit 126, and the coarse/fine switching signal is output with five bits in parallel to implement the bisection method. One example of the coarse/fine switching circuit 126 is shown in Figure 43.
15 The circuit comprises the window comparator of the fifth embodiment (Figure 28) and the bisection method control circuit (equivalent to the one shown in Figure 25) of the fourth embodiment.

Figure 44 shows a 13th embodiment. This embodiment
20 is a combination of the fifth embodiment (window comparator, Figure 27) and the seventh embodiment (history recording, Figure 33). The output of the comparator 22 and the monitor value and reference value to be supplied to the window comparator are coupled to
25 the coarse/fine switching circuit 128.

At start up, the sixth lowest bit of the counter is caused to count up or down until the monitor value is brought inside the level width of the window comparator, and then the third lowest bit of the counter is caused to
30 count up or down. After repeating the predetermined up/down pattern, the least significant bit is caused to count up or down repeatedly to stabilize the light output.

Figure 45 shows the detailed configuration of the
35 coarse/fine switching circuit 128. The circuit comprises the window comparator of the fifth embodiment (Figure 28) and the history recording shift register of the seventh

embodiment (Figure 34).

Figure 46 shows a coarse/fine switching circuit 230 used in a 14th embodiment. This embodiment is a combination of the eighth embodiment (history recording, Figure 37) and the fourth embodiment (bisection method, Figure 25). The output of the comparator is connected to the coarse/fine switching circuit 230. The coarse/fine switching circuit 230 comprises the history recording shift register of the eighth embodiment (Figure 34) and the bisection method coarse/fine control circuit (Figure 25).

Figure 47 shows a first example of the circuit configuration of the clock control circuit 72 used in each of the above-described embodiments other than the first embodiment.

In burst transmission, time intervals during which no data are transmitted are relatively long, and during these intervals, the light output value cannot be fed back. In view of this, the clock signals to be supplied to the counter 16, the coarse/fine switching circuit 26, 76, 82, 108, 116, 120, 124, 126, 128, or 230, and the D/A conversion circuit 14 are created from the input data and the base clock so that the counter will be updated only when there exists input data. The clock control circuit comprises a data detection circuit 232, a 4-bit binary counter 234, and a delay circuit 236. The data detection circuit 232 detects input data and produces a high output. Only when the output of the data detection circuit is high, and the carry of the 4-bit binary counter 234 is up (high), does the LOAD control input of the 4-bit binary counter go high, causing the data to be loaded into the 4-bit binary counter; thereafter, when the carry is cleared, the counter starts counting. The time chart shown in Figure 48 for the clock control circuit shows the setting in which a carry occurs when the data loaded into the 4-bit binary counter is "2" or when the count value is "1". The value of the most

significant bit, Q3, of the 4-bit binary counter is supplied as the counter clock signal.

The operation of the clock control circuit according to the present invention will be described with reference to Figures 47 and 48. First, the counter 234 is reset to zero by the reset signal and, when the count value becomes "1" at the next clock input, a carry occurs and the EN input of the counter 234 goes to the low level, so that the counting is stopped. Though the details of the data detection circuit 232 will be described later, when the data input to the data detection circuit 232 is "1" for three bits in succession, the output of the data detection circuit 232 goes high, and the value "2" is loaded into the counter 234. Thereupon, the counter 234 resumes counting; when the count value becomes "8", the output Q3 goes to the high level, and hence the counter clock is high. When the count value becomes 0, the output Q3 goes to the low level, so that the counter clock is low. When the count value becomes "1", a carry occurs, and the counter 234 stops. Thereafter, when the output of the data detection circuit 232 goes to the high level, the above process is repeated. A forced discharge signal (described later) is output from a flip-flop 238 in the delay circuit 236 with a delay of one clock relative to the counter clock. The D/A conversion clock is output by being delayed one more clock through a flip-flop 240.

In this way, the counter clock for defining the light output update timing is generated only when an input data signal occurs. That is, light output update timing synchronized to input data "1" can thus be realized.

One example of the data detection circuit 232 is shown in Figure 49. When an input data signal occurs for three bits in succession, all inputs to an AND gate 242 are 1s, so that the data detection output signal is high and the 4-bit binary counter starts counting. In this

example, an input data signal occurring for three bits in succession is detected, but this is not an essential condition.

5 The clock to be supplied to the D/A conversion circuit 14 is derived by delaying the output of the 4-bit binary counter 234 through the delay circuit 236 by considering the delay time through the counter 16 and the delay due to the input setup time, etc. of the D/A conversion circuit 14.

10 The forced discharge signal is used in the monitor section when it is needed to quickly lower the light output, for example, when starting control from an initial value higher than the target value. In the monitor section 70 shown in Figure 13, when the monitor
15 output is higher than the target value, the control value is reduced to lower the light output, and when the monitor current decreases, the monitor output gradually decreases due to the spontaneous discharge through the resistor 75. As a result, the monitor output may be
20 judged as being higher than the reference value when the light output is actually lower than the reference value, and the actual light output may be caused to drop far below the reference value. To address this problem, in the monitor section 243 shown in Figure 50, a transistor
25 244 is inserted in parallel with the resistor 75. At the completion of the updating of the counter 16, the transistor 244 is turned on by the forced discharge signal, forcing the charge on the capacitor 246 to be discharged. This improves the ability of the monitor
30 output to follow a rapid decrease in the light output. If the reference value for the light output control is to be generated from the data signal, a similar circuit can be used for the discharge of the reference value. Also, a conventional constant voltage circuit, such as the
35 previously described one, may be used as the reference value generating circuit.

When the initial value after clearing the digital

value by the reset signal is invariably lower than the light output reference value, and it is, therefore, not necessary to quickly reduce the light output, the forced discharge signal is not needed.

5 Furthermore, the monitor section and the reference value source may be constructed using a sample-and-hold circuit or an edge detection circuit that has neither a spontaneous discharge nor a forced discharge function.

10 In the above description, the update timing of the various output signals of the clock control circuit may be determined arbitrarily, considering the delay times, etc. of the various blocks implementing the light output control method of the present invention.

15 In the above embodiment, an external signal is used as the reset signal, but instead, use can also be made of a signal that a supply voltage detection circuit or the like (such as a conventional power-on reset circuit) automatically generates when a supply voltage is turned on. Furthermore, the reset signal may be generated using
20 a clock-off detection circuit that detects the absence of an input clock. Moreover, a combination of two or more of the external signal, the supply voltage detection circuit, and the clock-off detection circuit, may be used.

25 Figure 51 shows the detailed configuration of the counter 16 to explain how the initial value is loaded into the counter 16. The high-order five bits of the initial value are connected directly to the load data inputs of the high-order 5-bit up/down counter 38. The
30 low-order five bits are connected to one side of a five-gang switch 248. When the initial value load signal is high, the switch 248 selects the low-order five bits of the initial value for connection to the load data inputs of the up/down counter 36. When the initial value load
35 signal is low, the output of the comparator 22 is selected for connection to the load data inputs.

Figure 52 shows a second example of the clock

control circuit 72. To load the counter 16 with the initial value for the light output, the output signal from the data detection circuit is ORED with an initial value application end signal, and the result is input to
5 the LOAD terminal of the counter 234. With this arrangement, the counter clock is output at the end of the initial value application, as shown in Figure 53, and the initial value is loaded into the counter 16.

In the above-described example, light output update
10 timing synchronized to the input data "1" has been achieved, but it is also possible to generate light output update timing so that the digital value for light output is not updated by controlling the clock to be supplied to the counter 16, the coarse/fine switching
15 circuit, and the D/A conversion circuit only when there is no data. This can be achieved by the clock control circuit shown in Figure 54. The circuit comprises a data-off detection circuit, a 4-bit binary counter 234, and a delay circuit 236. The data-off detection circuit
20 250 detects input data "0" and produces a high output. The operation is the same as that described earlier, and if it is desired to add an initial value for the light output, as is done in Figure 52, the initial value application end signal may also be provided in Figure 54.
25 A specific example of the data-off detection circuit 250 is shown in Figure 55.

In the above description, the clock control circuit has been described as containing a delay circuit, but
30 combinational logic 252 may be used instead of the delay circuit. A specific example is shown in Figure 56.

Figure 57 shows an example of a clock control circuit in which a frequency divider is used instead of the counter. The counter 234 in Figure 47 is replaced by
35 a four-stage frequency divider 252, with the addition of a flip-flop 254 for synchronization with data detection. The data detection circuit 256 used here has the configuration shown in Figure 58. In Figure 58, when

there is no data, a transistor 258 is ON, and a capacitor 262 is charged with a current from a current source 260, increasing the voltage level of the capacitor 262. When there is data, a transistor 264 is ON, and the capacitor 262 is discharged through a current source 266, so that the voltage level decreases. A transistor 268 is OFF when its gate potential is high, causing the voltage detection output to go to the low level, and is ON when its gate potential is low, causing the detection output to go to the high level. That is, the detection output remains at the high level as long as there is data, and goes to the low level when there is no data. Figure 59 shows signals at points A to J in Figure 57.

Degradation mode of the laser diode (LD) will now be considered in connection with the negative feedback control in the light output control circuit. If the LD degrades due to aging, etc., its light-producing efficiency decreases and the monitor signal output from the photodiode (PD) drops. As a result, the digital value of the counter 16 for the light output continues to rise by the negative feedback control of the light output. Suppose here that, for any reason, the light-producing efficiency of the LD is restored; in that case, the digital value for the light output may have already risen to a maximum value. This could damage the LD.

The configuration shown in Figure 60 avoids the above LD damage by having the LD driving circuit 10 output an LD drive current limit signal to the counter 16 that controls the light output value, and thus stopping the light output increasing operation. Detailed circuit configurations of the LD driving circuit 10 and the counter 16 that controls the light output value are shown in Figures 61 and 62, respectively. In Figure 61, p-channel MOS transistors 60 and 62 and p-channel MOS transistors 60 and 270 respectively form current mirrors. Likewise, n-channel MOS transistors 272 and 274 and n-channel MOS transistors 56 and 58 respectively form

current mirrors. If the current IB generated by the transistors 60 and 270 is larger than the current IA (reference value) generated by a current source 276 and the transistors 272 and 274, the LD drive current limit signal goes high. The current IA generated by the current source 276 and transistors 272 and 274 provides the reference value below which the LD drive current is to be limited. When the limit signal is high, only the upward counting of the counter 38 shown in Figure 62 is disabled.

In the light output control circuit so far described, after the power up of the light output control circuit is completed and a steady state is reached, the light output value continually oscillates between two values around the reference value, as shown in Figure 63. Usually, the circuit is designed so that the two values come within the specified limits of the light output, but the light output value cycles through unnecessary changes.

Especially, in burst transmission, the time required for the light output to stabilize must be shortened; to achieve this, the feedback loop speed must be increased, but if the feedback is always performed at high speed, unnecessary updates will be repeated. This problem will result in increased error rate at the optical signal receiving end.

A problem associated with the D/A conversion circuit used in the above light output control circuit will be described with reference to Figure 64. When the light output control circuit updates its light output value, the digital code input to the D/A conversion circuit changes, and a spike called a glitch occurs at the output of the D/A conversion circuit. This glitch appears in the drive current, causing waveform distortion. This problem also results in increased error rate at the optical signal receiving end.

Figure 65 shows another embodiment of the present

invention, and Figure 66 illustrates its operation. This embodiment differs from the embodiments so far described in that, in addition to the clock control circuit 28 for controlling the clock supplied to the counter 16 that
5 stores the light output control value, an update permit control circuit 276 is provided that controls whether to permit or not permit the updating of the counter 16. The counter update permit control is performed by issuing an update permit signal SIG1 from the update permit control
10 circuit 276. Once the counter 16 has been updated in response to the signal SIG1, unnecessary updating is prohibited for a time longer than the minimum necessary cycle for updating by the feedback, by not permitting updating until a prescribed condition is satisfied by a
15 count of the clock or data signal, etc. This serves to reduce the number of unnecessary updates by lengthening the actual feedback cycle. Though the light output oscillates between the two values around the reference value, its frequency can be reduced and the waveform can
20 thus be improved.

In the example of Figure 65, the logic state of SIG1 is "1" = High when permitting an update, and "0" = Low when prohibiting updates. After an update, the state goes to "0", and this state is maintained until a
25 prescribed condition is satisfied; after the condition is satisfied, the state remains at "1" until the next update is performed. Several examples will be given later, dealing with a specific method of generating the signal SIG1.

In the circuit of Figure 65, the update permit control signal, generated separately from the clock supplied to the counter 16, is used for counter
30 update/prohibit control; alternatively, logic operations may be performed between the permit signal and the clock, with provisions made to stop the clock itself when
35 prohibiting updates (this can be easily accomplished using an AND gate, etc.). In that case also, exactly the

same effect can be achieved. The following description deals with the update permit signal independent of the clock, but it is self-evident that the same thing can also be achieved using the method of stopping the clock
5 itself.

Next, still another embodiment of the present invention will be described with reference to Figures 67 and 68. This embodiment achieves high-speed updating during power up, while reducing the number of light
10 output updates once the control reaches a steady-state condition.

The operation of this embodiment is shown in Figure 67. High-speed power up and the reduction of waveform degradation during steady-state control are
15 simultaneously achieved by using a switching signal SIG2 and switching the mode between a power-up mode in which feedback is performed with the minimum necessary cycle for updating and a steady-state mode in which, once an update is done, updating is prohibited until a prescribed
20 condition is satisfied. In the illustrated example, SIG2 remains at "1" during the high-speed power up, and goes to "0" when steady state is reached.

Figure 68 shows the configuration for implementing the above operation. An operation mode switching section
25 for generating the signal SIG2 indicating the power-up mode is added in the circuit of Figure 65, and SIG2 and the output of the update permit control circuit 276 are ORed by an OR gate 279, and the result is input as SIG1 to the counter 16. The switching signal SIG2 can be
30 generated from the data, clock, or other external signal, and several examples will be given later to explain a specific method of signal generation.

A further embodiment of the present invention will be described with reference to Figure 69. This
35 embodiment is intended, while retaining the high-speed power up function, to prevent the degradation of the light output waveform caused by glitches occurring in the

D/A conversion circuit when updating the light output control value.

5 The basic configuration of Figure 69 is the same as that of Figure 68, the only difference being that the frequency band of the current source that determines the drive current in the LD driving circuit is made switchable as the operation mode is switched from the high-speed power up mode to the steady-state mode.

10 More specifically, for power up, the frequency band of the current source is widened and the feedback speed increased so that the light output quickly rises to the target value, thus achieving high-speed power up, and after steady state is reached, the feedback speed is reduced and the frequency band of the drive current
15 narrowed to prevent the degradation of the light waveform due to glitches in the D/A conversion circuit, thus enabling communications to be performed with good light waveform.

20 Figure 70 shows an example of the update permit control circuit 276. To limit the update frequency, after the counter 16 that stores the light output control value has been updated, a digital timer for counting the clock is started to prohibit updating for a predetermined period of time, after which the updating is permitted.

25 The circuit operation will be described below. At first, a clock derived by dividing the base clock by two using a frequency divider 282 is input to the counter 280, but because Q0 to Q7 are loaded with 11111111 (binary number representing the decimal number 255) and the carry CO is set to "1", setting the enable E to "0",
30 the counter 280 is disabled. In this condition, when a counter clock is input, a D-FF detects the rising of the counter clock and loads 0 into the counter 280. This forces the carry CO to go to "0", and the counter state
35 changes from the disabled state to the count enabled state. The counter 280 counts up by 1 by the divide-by-two derived clock. At this time, if the counter clock

changes again, the change is ignored because "0" is applied to the LOAD terminal of the counter 280 by the state of the carry CO. As a result, the counter 280 continues to count up until counting up to 255 (decimal).
5 When the value of the counter 280 reaches 255 (decimal), the carry CO goes to "1", setting the enable E to "0", so that the counter 280 is stopped. When the next counter clock is input, the above process is repeated. With the above operation, once the counter clock is input, SIG1 is
10 held at the low level to prohibit the updating of the counter 16 until after the base clock is input $2 \times 256 = 512$ times. After that, updating is permitted. For example, when the base clock rate is 156 Mb/s, and when the counter clock is continuously input, updating is
15 permitted once every $3.3 \mu\text{s}$ ($6.43 \text{ ns} \times 512$).

Figures 71 and 72 shows detailed circuit diagrams of the LD driving circuit 10. Figure 71 shows the circuit when the analog output of the D/A conversion circuit is given as a voltage, and Figure 72 shows the circuit when
20 the analog output is given as a current. Except that a band switching circuit 284 is inserted between the transistors 60 and 62, the circuit configuration is fundamentally the same as that of the voltage input/current input LD driving circuit described with
25 reference to Figure 11.

Figure 73 shows a circuit diagram of the band switching circuit, and Figure 74 shows its operational sequence. This circuit switches the frequency band for the current output of the LD driving circuit by using an
30 operation switching signal.

The transistors 60 and 62 at left and right form a current mirror as a current source for determining the drive current. The current proportional to the analog output of the D/A conversion circuit is input to the
35 transistor 60, and the output current is taken from the transistor 62.

The basic principle of band switching is to switch an RC-type low-pass filter consisting of RN3 and CN3 in and out of the path connecting between the two transistors 60 and 62. Further, when switching in the capacitor C, if the capacitor with a different potential is switched in abruptly, a charge current will flow momentarily, as a result of which the gate may become unstable, disrupting the output current waveform. To address this, a circuit is provided that makes the potential of CN3 the same as the gate potential. To accomplish such switching operation, SW1 to SW3 and a sequence control circuit for proper operation of these switches are included.

A description will be given below of how the switching is made from the high-speed power up mode in which the frequency band of the current mirror is made wide to the steady-state mode in which the frequency band is made narrow.

In the high-speed start up mode, a wide frequency band is achieved with SW1 = ON, SW2 = OFF, and SW3 = ON. Since the gates of the transistors 60 and 62 are short-circuited via the switch SW1, and CN3 is not connected to the gate of the transistor 62, the transistors 60 and 62 form a normal current mirror configuration, and the frequency band is therefore wide.

The p-channel MOS transistor MM1 of the same size as the transistor 62 also forms a current mirror with the transistor 60, and a current equivalent to that of the transistor 62 flows therein. Further, the current of MM1 flows to the n-channel MOS transistor MM2, and the current flowing in MM3 which forms a current mirror with MM2 flows to MM4, so that the gate level of MM4 becomes equal to that of the transistor 62. At this time, since SW1 is ON and SW2 OFF, CN3 is charged to the same voltage level as the gate voltage of the transistor 62.

When the switching signal changes from "1" to "0", SW1 is opened and the capacitor CN3 is released; after

that, N1 changes from "0" to "1" via an inverter and an RC time constant circuit consisting of CN1 and RN1, and SW2 is closed to connect CN3 to the gate of the transistor 62.

5 After N1 changes from "0" to "1", N2 changes from "1" to "0" via an inverter and an RC time constant circuit consisting of CN2 and RN2; as a result, SW3 short-circuiting across RN3 is opened, thus inserting RN3 between the gates of the transistors 60 and 62, and the
10 low-pass filter consisting of RN3 and CN3 is thus switched in between the gates of transistors 60 and 62.

 In this way, the band switching circuit can switch the frequency band by switching the low-pass filter in and out of the current mirror that controls the drive
15 current.

 While the above-described band switching circuit is designed to insert an RC time constant circuit, the band switching circuit shown in Figure 75 is designed to add RN3 only. The band switching circuit section consists
20 only of the resistor RN3 shown in Figure 73 and a circuit that controls the insertion of RN3. Since each of the transistors forming the circuit has a capacitive component, band switching can be accomplished by connecting and disconnecting only R.

25 The band switching circuit shown in Figure 76 is designed to add CN3 only. The band switching circuit section consists only of the capacitor CN3 shown in Figure 73 and a circuit that controls the insertion of CN3. Since each of the transistors forming the circuit
30 has a resistive component or a current limiting function as a current source, band switching can be accomplished by connecting and disconnecting only C.

 The signal that the coarse/fine switching circuit 26 described with reference to Figure 7 outputs can be used
35 directly as the operation switching signal SIG2 for switching the operation mode between the start-up mode in which the update cycle is short and the steady-state mode

in which the update cycle is long, or for switching the frequency characteristics of the LD driving circuit, or for both switching operations. Alternatively, the circuit 26 of Figure 7 can be used as a coarse/fine switching and operation mode switching circuit that outputs coarse/fine switching and operation mode switching signals for coarse/fine switching and operation mode switching, as shown in Figure 77.

Likewise, the coarse/fine switching circuit 76 shown in Figure 18, the coarse/fine switching circuit 82 shown in Figure 25, the coarse/fine switching circuit 88 shown in Figure 28, the coarse/fine switching circuit 108 shown in Figures 34 and 35, and the coarse/fine switching circuit shown in Figure 37 can each be used as the operation mode switching circuit or the coarse/fine switching and operation mode switching circuit. The circuits implementing the latter example are shown in Figures 78 to 82, respectively. Alternatively, provisions may be made to externally apply the operation mode switching signal or the coarse/fine switching and operation mode switching signal, as shown in Figure 83.

Another example of the coarse/fine switching and operation mode switching circuit is shown in Figure 84. This circuit, using an analog circuit, detects a change in the comparator output and generates the switching signal. A same-sign succession detection circuit using a charge pump is contained for detecting a change in the comparison result.

The charge pump circuit 286 comprises: a capacitor C1; M1 capable of outputting a constant current I1 using a constant current source I1 and a p-channel MOS FET M2; M3 capable of performing a switching operation in response to an input signal; M5 capable of outputting a constant current I2 using a constant current source I2 and an n-channel MOS FET M6; M4 capable of performing a switching operation in response to an input signal; and an n-channel MOS FET M7 which is turned on when the reset

signal is low, to discharge the capacitor C1.

The charge pump control circuit 288 has the following three functions.

When the comparator output is "1" = UP, control is performed so that when the counter clock goes high (for counter updating), M3 is turned on to discharge the capacitor C1; as a result, the output VC of the charge pump circuit is lowered toward ground.

When the comparator output is "0" = DOWN, control is performed so that when the counter clock goes high (for counter updating), M4 is turned on to charge the capacitor C1; as a result, the output VC of the charge pump circuit is raised toward Vdd.

When the reset signal RST is low, M7 is turned on to short the output VC of the charge pump circuit to ground, thereby providing an initial value to C1.

A level comparator 289 includes a resistive voltage dividing circuit for dividing the voltage between the power supply Vdd and ground GND using resistors R1 to R3, and detects the mixing of UP control and DOWN control by detecting the output VC of the charge pump circuit falling within a range of $R1/(R1+R2+R3)$ to $(R1+R2)/(R1+R2+R3)$ (when Vdd = 3 V and $R1 = R2 = R3 = 5\text{ k}\Omega$, then VC = 1 to 2 V) by using two differential comparators and an OR circuit.

Figure 85 shows the operation of the switching circuit of Figure 84. When the reset signal RESET goes high, M7 is turned on and the charge pump circuit starts operating. During initial power up of the light output control circuit, when the light output is smaller than the reference value, the comparator output is "1" = UP; in this state, when the counter clock goes high (for counter updating), M3 is turned on to discharge the capacitor C1, so that the output VC of the charge pump circuit remains at GND.

Then, when the light output reaches the reference value, and the comparator output begins to cycle between

"1" = UP and "0" = DOWN, the ON frequency of M3 increases and the capacitor C1 is discharged, so that the output VC of the charge pump circuit takes a value intermediate between Vdd and GND. As a result, the output of the level comparator 289 goes high. The latch 290 at the final stage is provided to permit the power-up operation only once after releasing the reset state.

Figure 86 shows another example of the update permit control circuit 276. The difference from the example of Figure 70 is that while in Figure 70 the base clock is directly input to the frequency divider 282, in Figure 86 the base clock is ANDed with the data and the result is input to the frequency divider 282. That is, in the update permit control circuit of Figure 70, the period from an update permit to the next update permit (update prohibit period) is determined by counting the base clock, but in the update permit control circuit of Figure 86, the update prohibit period is determined by counting the number of 1s occurring in the data. For continuous transmission, both circuits operate substantially the same, but for burst transmission, the prohibit period becomes long during no-cell intervals according to the circuit of Figure 86.

Still another example of the update permit control circuit 276 is shown in Figure 87. To limit the update frequency, the circuit counts the difference between the number of times that the result of the comparison between the monitor value and the reference value indicates UP and the number of times that the result of the comparison indicates DOWN, and prohibits updating until the resultant value settles to a prescribed value. In the illustrated example, this corresponds to the time when a carry occurs with the counter counting up to the prescribed value 11111111 (255 in decimal). When the result of the comparison begins to cycle between UP and DOWN, this means that the light output is nearing the target value. At this time, the count changes up and

down around the target value, holding the counter value within a specified limited range, thus preventing unnecessary updates.

5 Figure 88 is a timing chart showing the operation of the circuit of Figure 87. During the period that the switching signal SIG2 is held at the high level, SIG1 is high and the counter 16 is updated in response to the counter clock. After that, the counter 16 is updated only when the value of the counter 292 reaches a maximum value +255 or a minimum value +0. The number 128 is
10 loaded when the value of the counter 292 has reached +255 or +0.

 Figure 89 shows a further example of the update permit control circuit 276. In this example, the number
15 of UP controls and the number of DOWN controls in the monitor/reference value comparison result history are counted by counters 294 and 296, respectively, and an update is performed when one or the other of the numbers exceeds a predetermined value. Figure 90 shows the
20 operation of the update permit control circuit of Figure 89.

 Figure 91 shows a still further example of the update permit control circuit 276. In this example, an
25 update is performed for each transmission of a cell by using a signal indicating the presence or absence of a burst cell. This serves to limit the number of updates. Figure 92 shows the operation of this update permit control circuit. In burst transmission, a burst cell
30 signal indicating a cell presence time segment is sent out from the apparatus; using this signal, the number of updates can be reduced during steady-state control. For this purpose, the operation switching signal SIG2, burst cell signal, and counter clock are input to the update permit control circuit. In the high-speed power up
35 operation mode, the update permit control signal SIG1 is set to "1", and in the steady-state mode, "1" = UPDATE PERMIT is output when the burst cell signal goes to "1"

and, at the next counter clock input, "0" = PROHIBIT is output. Since the number of updates can be reduced, the above operation has the effect of improving the waveform.

CLAIMS

1. A light output control circuit comprising:
 - a photodetector which detects the light output of a light-emitting device;
 - 5 a comparator which compares a light output detection value with a reference value;
 - a light output control device which controls the light output of said light-emitting device in a discrete manner in accordance with the result of
 - 10 said comparison output from said comparator; and
 - a switching circuit which counts the number of control actions performed by said light output control device, and which instructs said light output control device to perform control in accordance with a
 - 15 power-up mode until the number of control actions after starting the control reaches a predetermined value, and to perform control in accordance with a steady-state mode after the number of control actions has reached said predetermined value.
- 20 2. A light output control circuit according to claim 1, further comprising a clock control circuit which detects data to be supplied to said light-emitting device, generates a clock in accordance with the result of said detection, and supplies said clock as a timing
- 25 signal indicating control timing to said light output control device and said switching circuit.
3. A light output control circuit according to claim 2, wherein said switching circuit sets the amount of change of a control value per control action in said
- 30 light output control device in said power-up mode to a first amount of change, and sets the amount of change of the control value per control action in said light output control device in said steady-state mode to a second amount of change that is smaller than said first amount
- 35 of change.
4. A light output control circuit according to claim 3, wherein said switching circuit incrementally

reduces said first amount of change in said power-up mode over a plurality of stages.

5 5. A light output control circuit according to claim 4, wherein said first amount of change is reduced using a bisection method.

 6. A light output control circuit according to claim 5, further comprising an update permit control circuit which permits said light output control device to update said control value in a prescribed cycle in said
10 steady-state mode.

 7. A light output control circuit according to claim 6, wherein a frequency band of a drive current for said light-emitting device is set narrower in said steady-state mode than in said power-up mode.

15 8. A light output control circuit comprising:
 a photodetector which detects the light output of a light-emitting device;
 a comparator which compares a light output detection value with a reference value;
20 a light output control device which controls the light output of said light-emitting device in a discrete manner in accordance with the result of said comparison output from said comparator; and
 a switching circuit which instructs said
25 light output control device to perform control in accordance with a power-up mode until said light output detection value, after starting the control, enters a window of a prescribed width, and to perform control in accordance with a steady-state mode after said detection
30 value has entered said window.

 9. A light output control circuit according to claim 8, wherein the width of said window varies depending on temperature.

35 10. A light output control circuit comprising:
 a photodetector which detects the light output of a light-emitting device;
 a comparator which compares a light output

detection value with a reference value;

a light output control device which controls the light output of said light-emitting device in a discrete manner in accordance with the result of said comparison output from said comparator; and

a switching circuit which instructs said light output control device to perform control in accordance with a power-up mode until a control history of said light output control device, after starting the control, matches a prescribed pattern, and to perform control in accordance with a steady-state mode after said control history has matched said prescribed pattern.

11. A light output control circuit comprising:

a photodetector which detects the light output of a light-emitting device;

a comparator which compares a light output detection value with a reference value;

a light output control device which controls the light output of said light-emitting device in a discrete manner in accordance with the result of said comparison output from said comparator; and

a clock control circuit which detects data to be supplied to said light-emitting device, generates a clock in accordance with the result of said detection, and supplies said clock as a timing signal indicating control timing to said light output control device.

12. A light output control circuit according to claim 11, wherein said clock control circuit includes:

a data detection circuit which detects the data to be supplied to said light-emitting device;

a counter which outputs as said timing signal one of a plurality of bit outputs indicating a count value, and which stops counting when a carry or a borrow occurs in said count value; and

a gate circuit which applies a load signal for loading a prescribed value into said counter when a carry or a borrow occurs in said counter and when said

data detection circuit detects said data.

13. A light output control circuit comprising:

a photodetector which detects the light output of a light-emitting device;

5 a comparator which compares a light output detection value with a reference value;

a light output control device which controls the light output of said light-emitting device in a discrete manner in accordance with the result of said comparison output from said comparator; and

10 an update permit control circuit which, after said light output has stabilized, prohibits updating of a control value for said light output from the time that said control value is last updated, until the time that a prescribed condition is satisfied.

14. A light output control circuit according to claim 13, wherein said update permit control circuit permits the next update after a predetermined time has elapsed from the last update of said control value.

20 15. A light output control circuit according to claim 13, wherein said update permit control circuit permits the next update after data has been applied to said light-emitting device a predetermined number of times since the last update of said control value.

25 16. A light output control circuit according to claim 13, wherein said update permit control circuit permits updating of said control value when the difference between the number of times the output of said comparator has indicated that said control value should be increased and the number of times the output of said comparator has indicated that said control value should be decreased has reached a predetermined value.

30 17. A light output control circuit according to claim 13, wherein said update permit control circuit permits updating of said control value when either the number of times the output of said comparator has indicated that said control value should be increased or

the number of times the output of said comparator has indicated that said control value should be decreased has reached a predetermined value.

- 5 18. A light output control circuit according to claim 13, wherein said update permit control circuit permits updating of said control value in accordance with a signal indicating a burst transmission.

- 10 19. A light output control circuit comprising:
 a photodetector which detects the light
 output of a light-emitting device;
 a comparator which compares a light output
 detection value with a reference value; and
 a light output control device which
15 controls the light output of said light-emitting device
 in a discrete manner in accordance with the result of
 said comparison output from said comparator, wherein
 after said light output has stabilized, a
 frequency band of a drive current for said light-emitting
 device is reduced in width.

LIGHT OUTPUT CONTROL CIRCUIT

5

ABSTRACT OF THE DISCLOSURE

Using a switching signal from a coarse/fine
switching and operation mode switching circuit, the width
10 of change of a counter control value during power up is
increased, and the width of change is reduced once a
steady state is reached. In the steady state, the
frequency of updating is limited by a control signal from
an update permit control circuit. In the steady state,
15 the frequency band of a current source in an LD driving
circuit is reduced in width.

Fig. 1

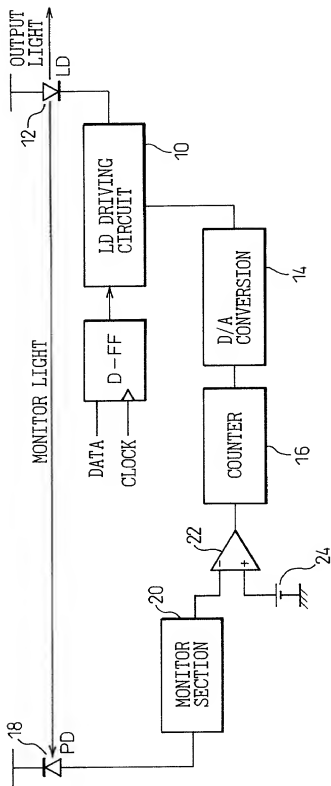


Fig. 2

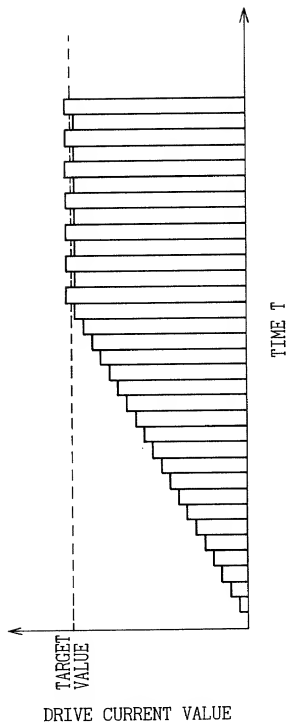


Fig. 3

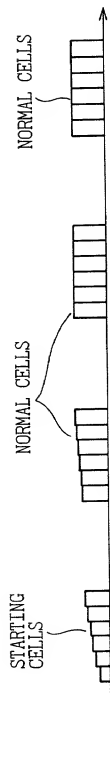


Fig. 4

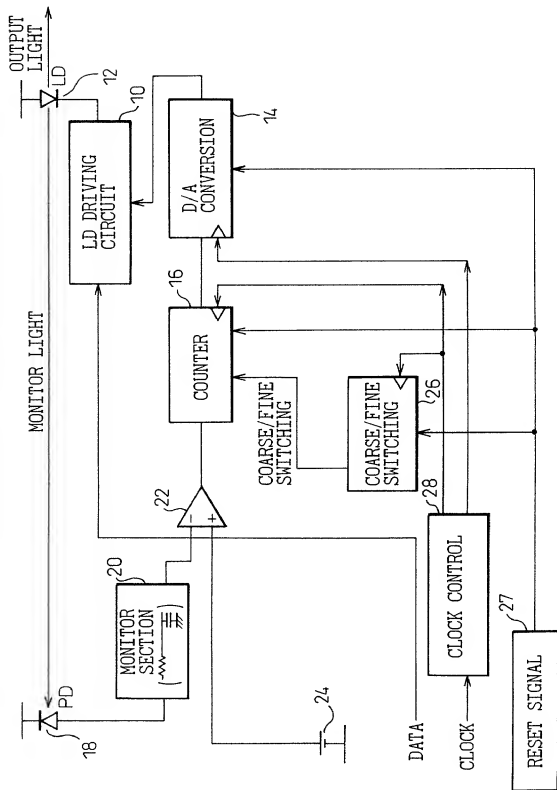


Fig. 5

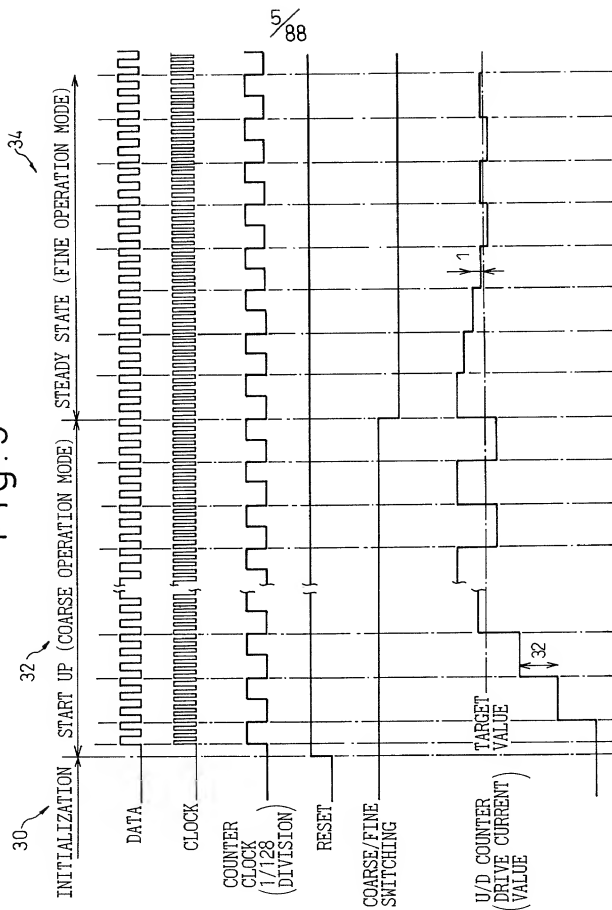


Fig. 6

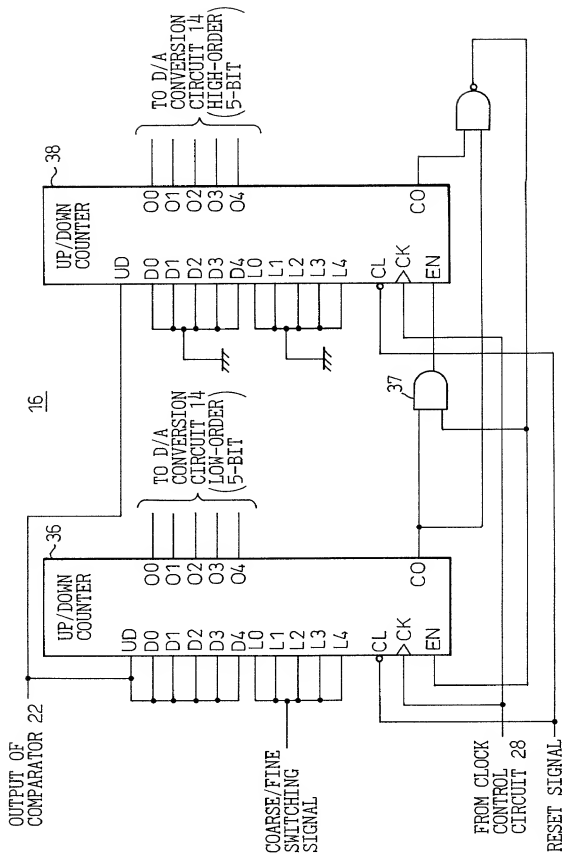


Fig.7

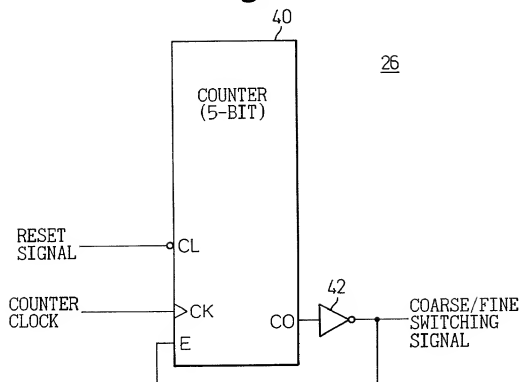


Fig.8

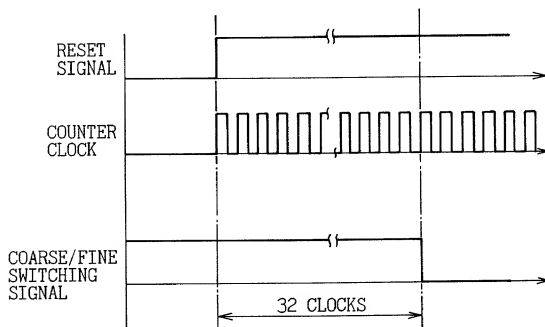


Fig. 9

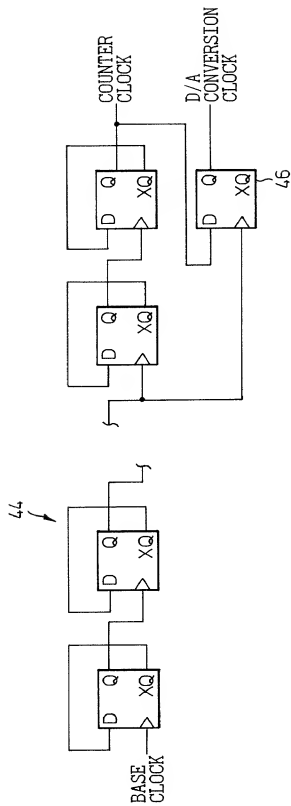


Fig.10

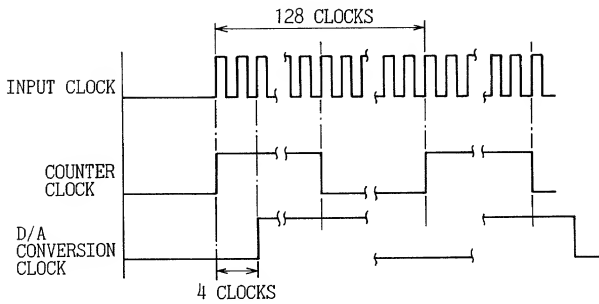


Fig.11

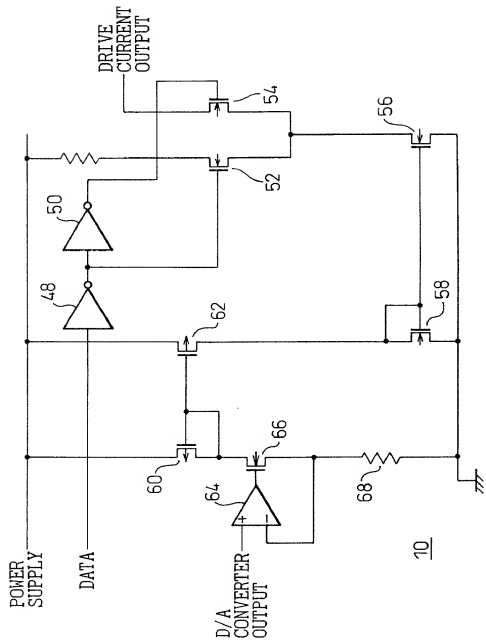


Fig. 12

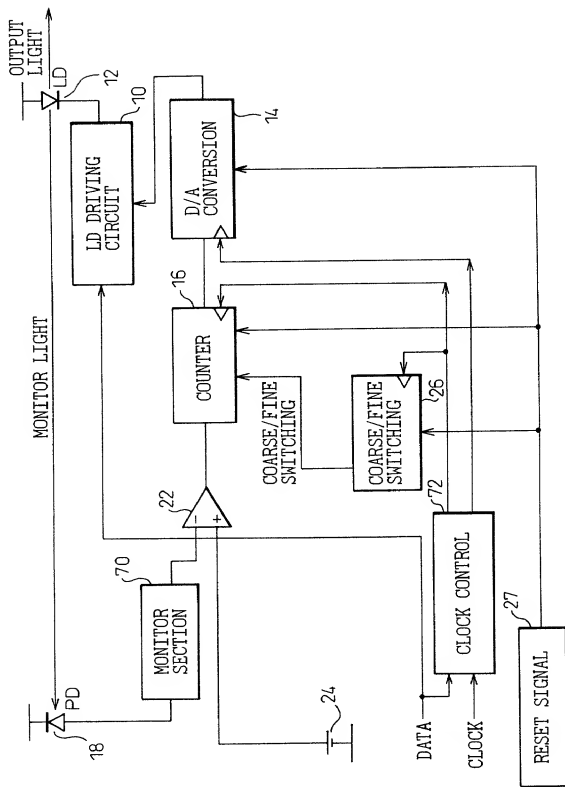


Fig. 13

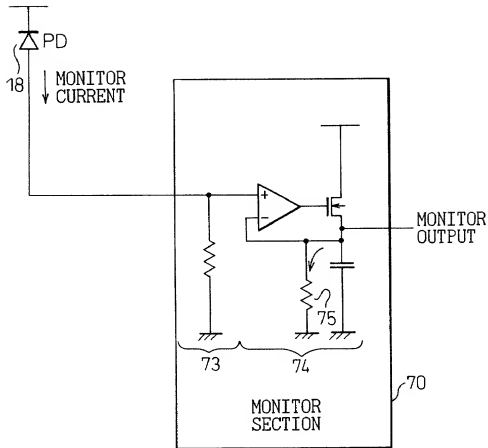


Fig. 14

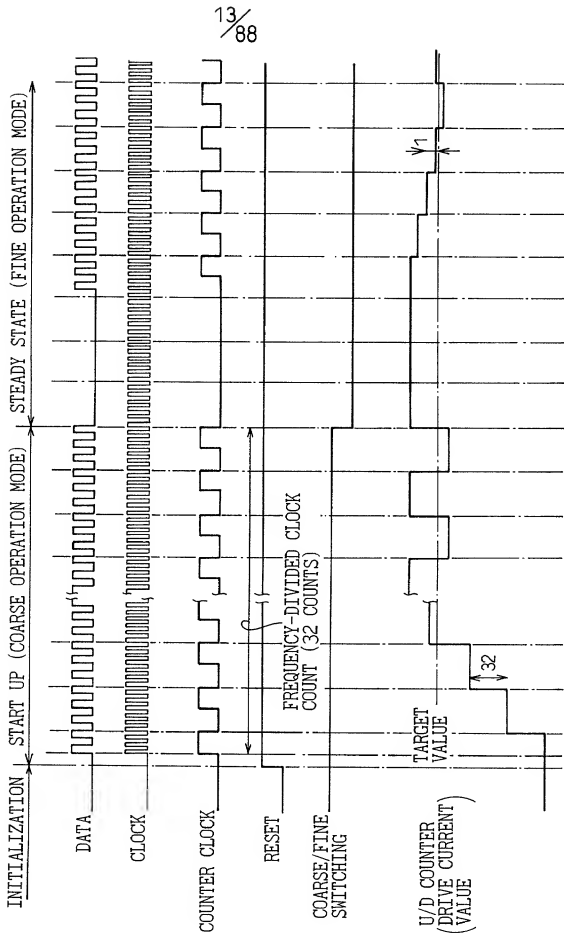
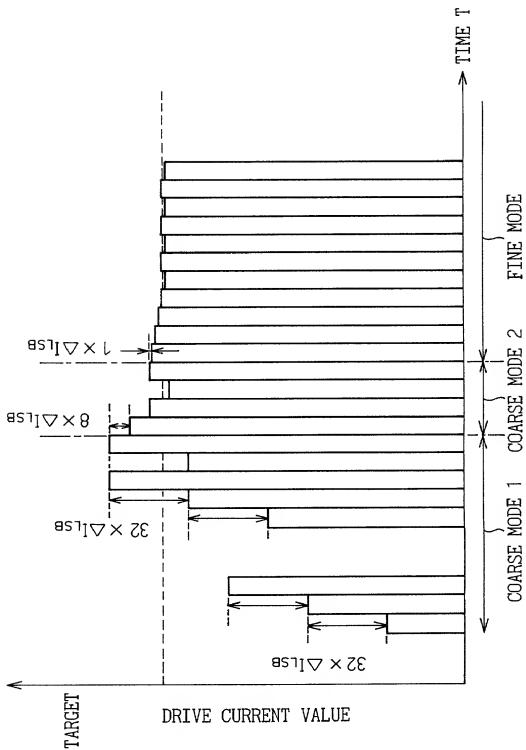


Fig. 15



1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100	2101	2102	2103	2104	2105	2106	2107	2108	2109	2110	2111	2112	2113	2114	2115	2116	2117	2118	2119	2120	2121	2122	2123	2124	2125	2126	2127	2128	2129	2130	2131	2132	2133	2134	2135	2136	2137	2138	2139	2140	2141	2142	2143	2144	2145	2146	2147	2148	2149	2150	2151	2152	2153	2154	2155	2156	2157	2158	2159	2160	2161	2162	2163	2164	2165	2166	2167	2168	2169	2170	2171	2172	2173	2174	2175	2176	2177	2178	2179	2180	2181	2182	2183	2184	2185	2186	2187	2188	2189	2190	2191	2192	2193	2194	2195	2196	2197	2198	2199	2200	2201	2202	2203	2204	2205	2206	2207	2208	2209	2210	2211	2212	2213	2214	2215	2216	2217	2218	2219	2220	2221	2222	2223	2224	2225	2226	2227	2228	2229	2230	2231	2232	2233	2234	2235	2236	2237	2238	2239	2240	2241	2242	2243	2244	2245	2246	2247	2248	2249	2250	2251	2252	2253	2254	2255	2256	2257	2258	2259	2260	2261	2262	2263	2264	2265	2266	2267	2268	2269	2270	2271	2272	2273	2274	2275	2276	2277	2278	2279	2280	2281	2282	2283	2284	2285	2286	2287	2288	2289	2290	2291	2292	2293	2294	2295	2296	2297	2298	2299	2300	2301	2302	2303	2304	2305	2306	2307	2308	2309	2310	2311	2312	2313	2314	2315	2316	2317	2318	2319	2320	2321	2322	2323	2324	2325	2326	2327	2328	2329	2330	2331	2332	2333	2334	2335	2336	2337	2338	2339	2340	2341	2342	2343	2344	2345	2346	2347	2348	2349	2350	2351	2352	2353	2354	2355	2356	2357	2358	2359	2360	2361	2362	2363	2364	2365	2366	2367	2368	2369	2370	2371	2372	2373	2374	2375	2376	2377	2378	2379	2380	2381	2382	2383	2384	2385	2386	2387	2388	2389	2390	2391	2392	2393	2394	2395	2396	2397	2398</
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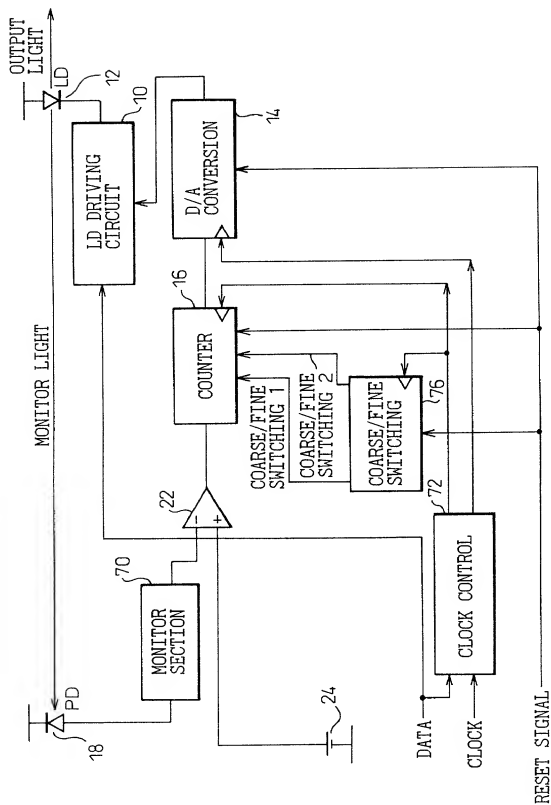


Fig. 17

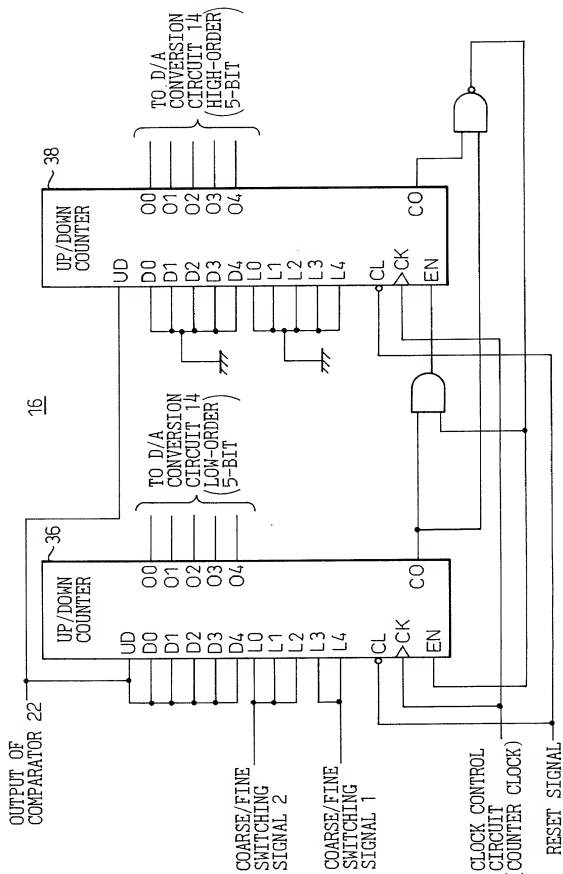


Fig.18

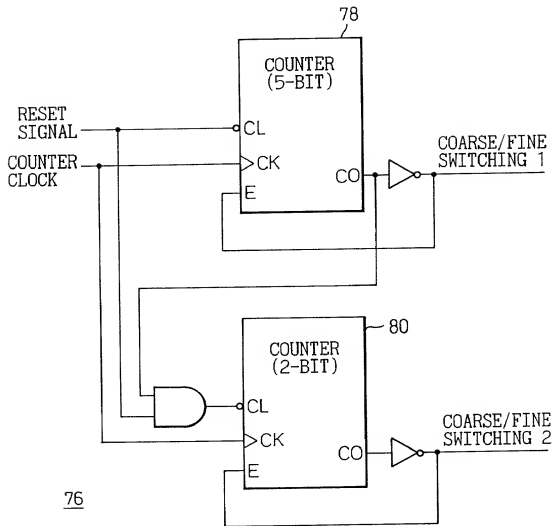


Fig.19

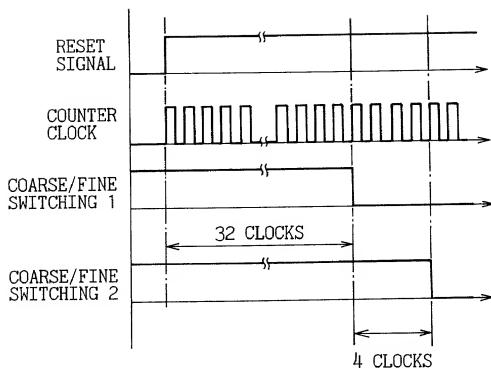


Fig.20

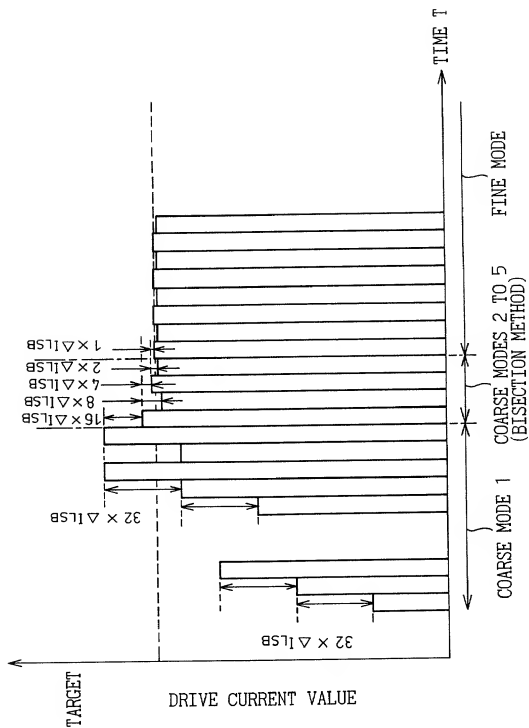


Fig. 21

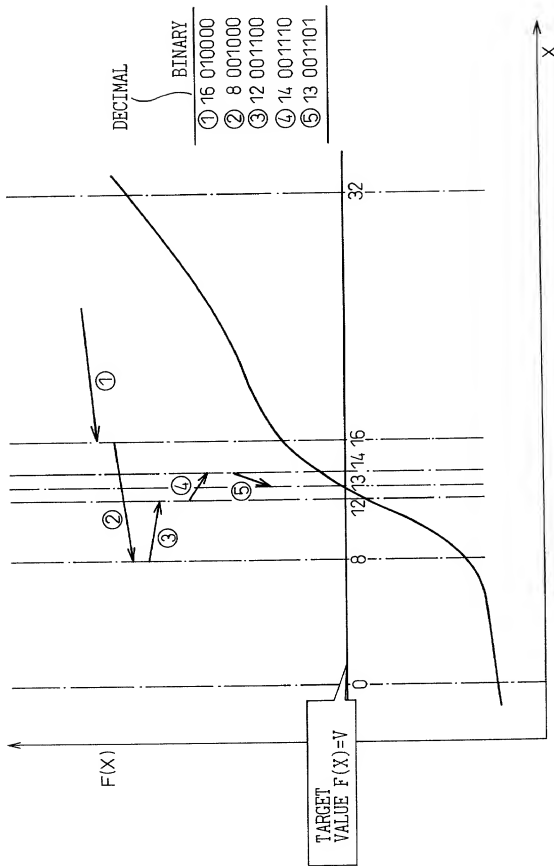


Fig. 22

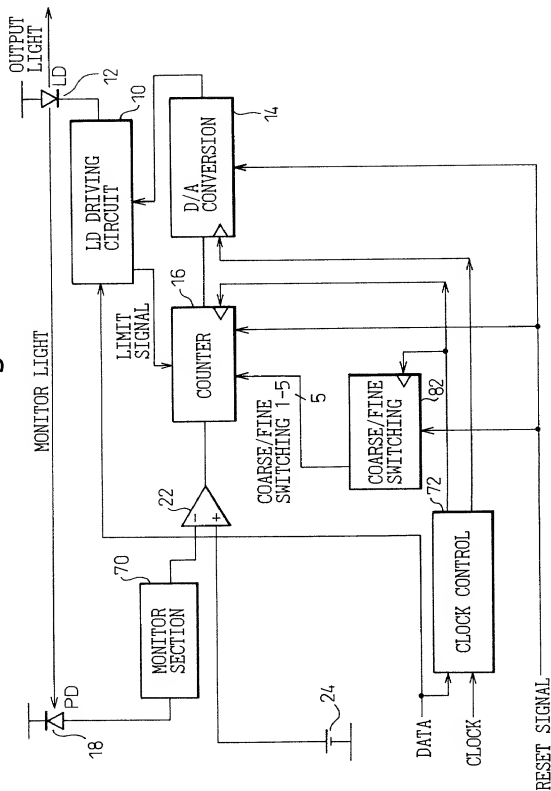


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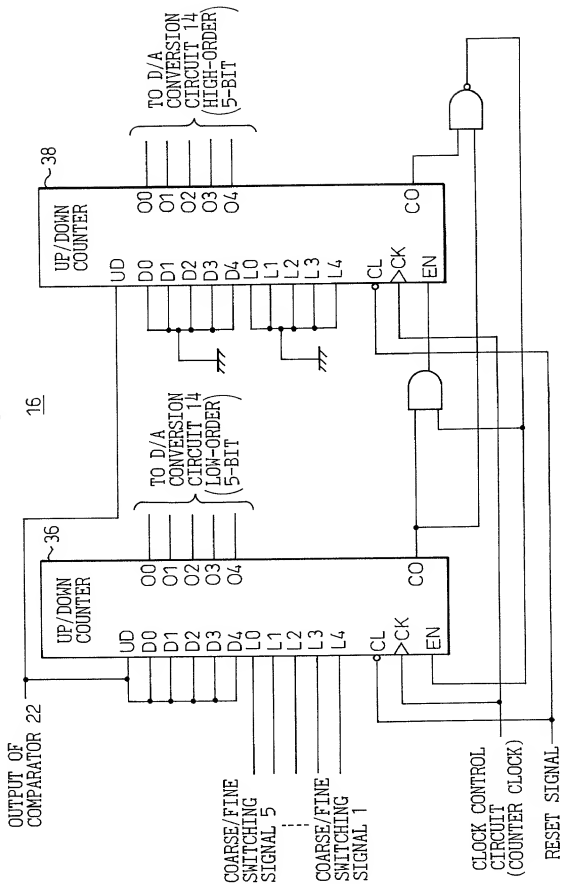


Fig.24

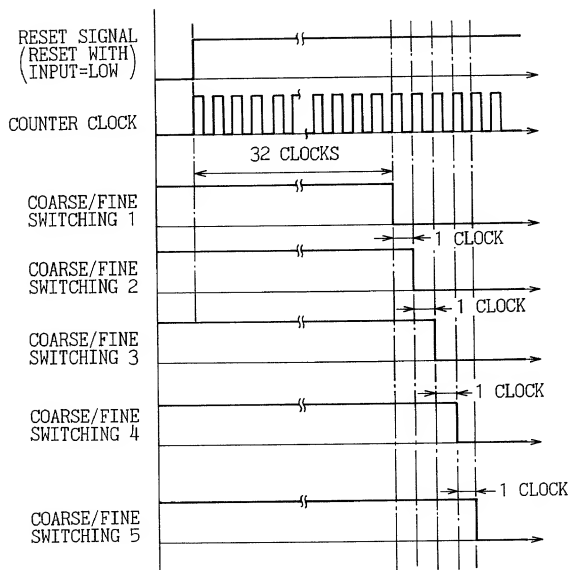


Fig. 25

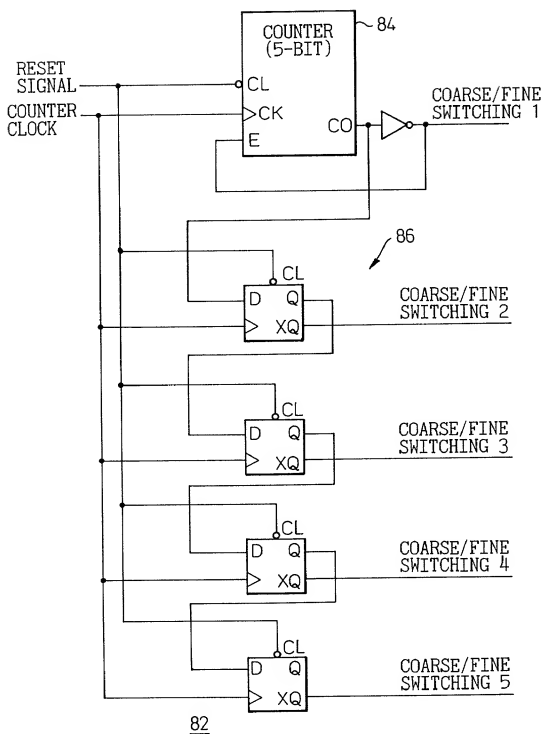


Fig. 26

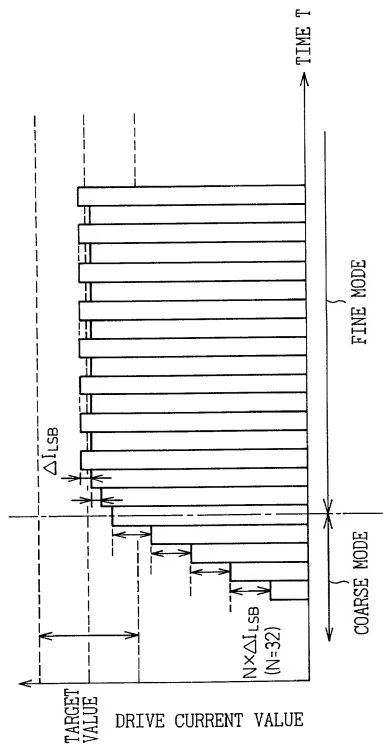


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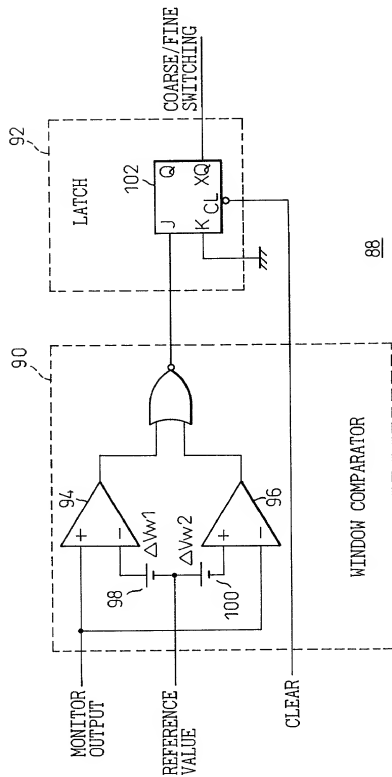


Fig. 29

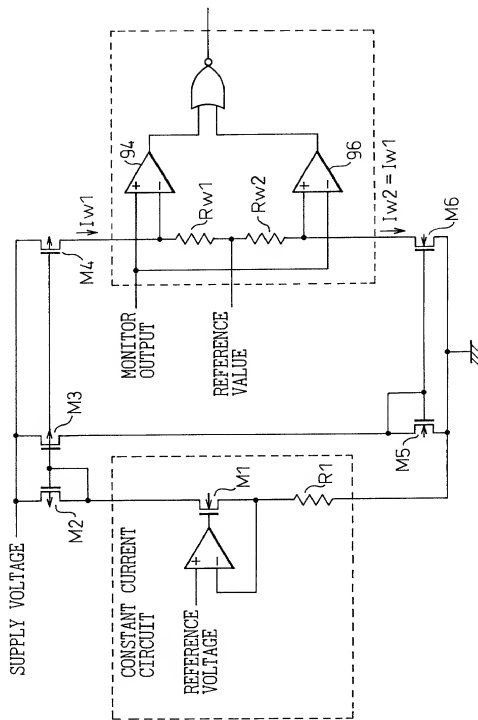


Fig.30

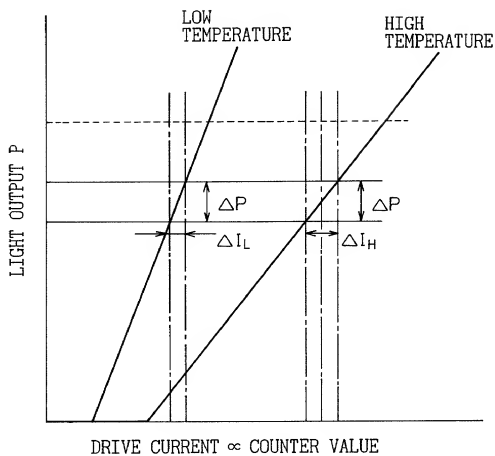


Fig.32

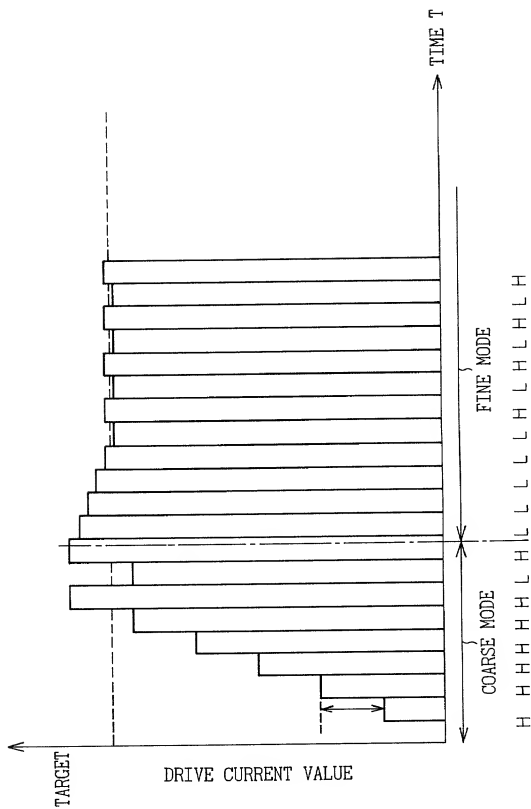


Fig. 33

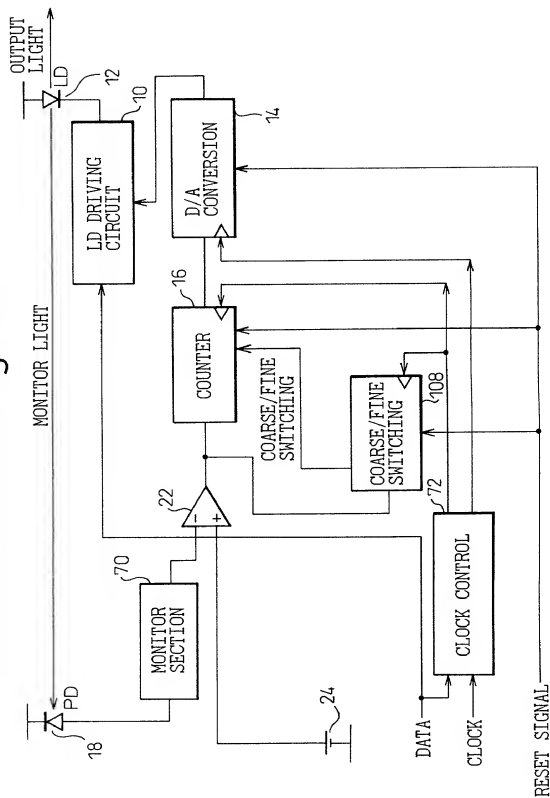


Fig. 34

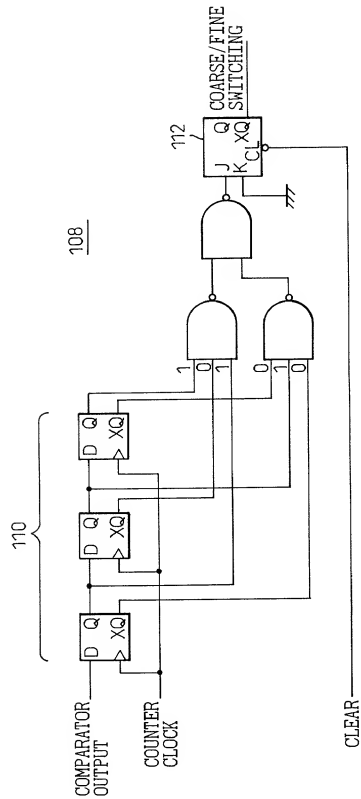
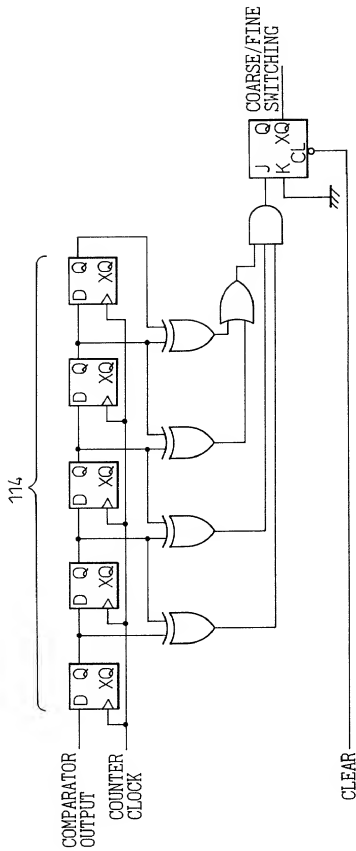


Fig.35



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Fig. 36

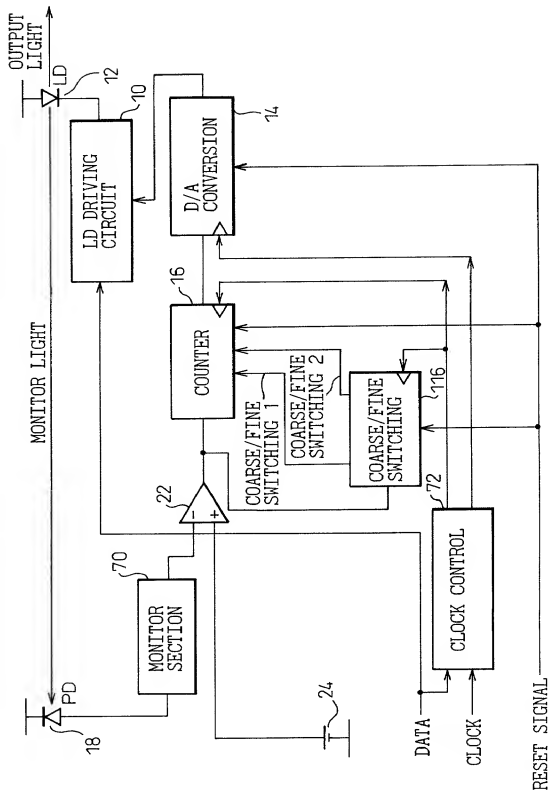


Fig. 37

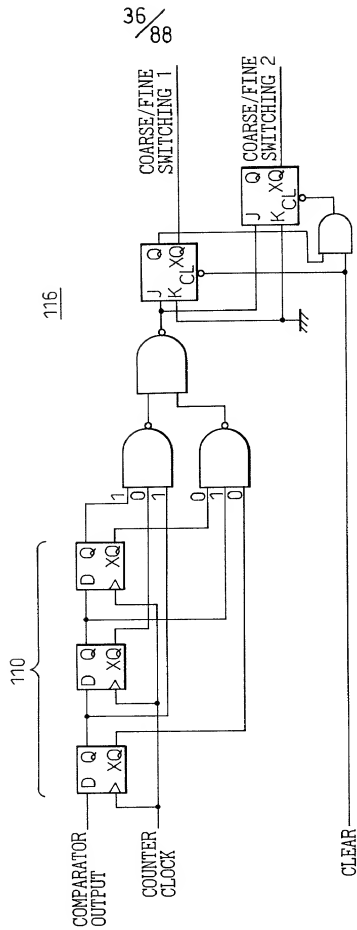


Fig.38

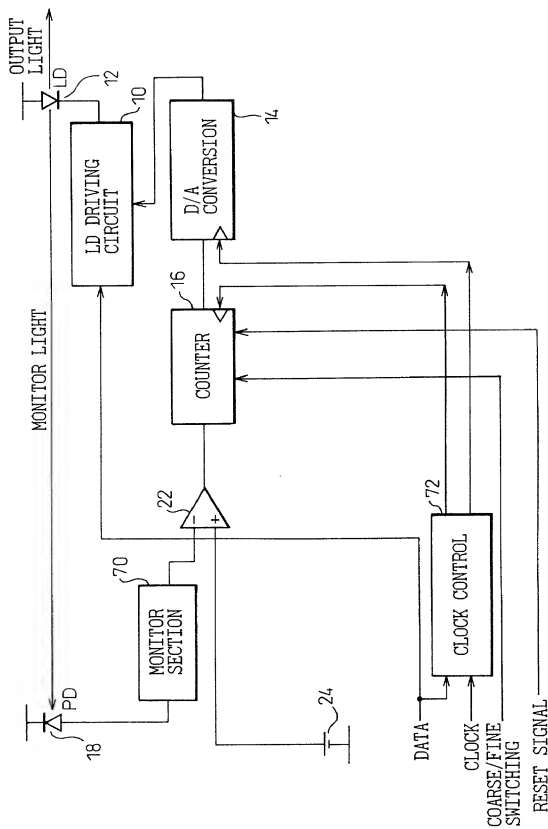


Fig.39

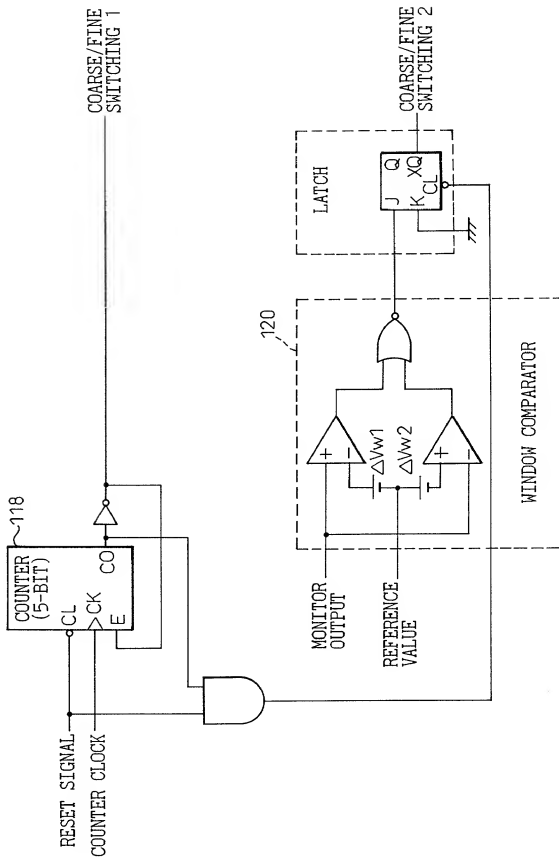


Fig. 40

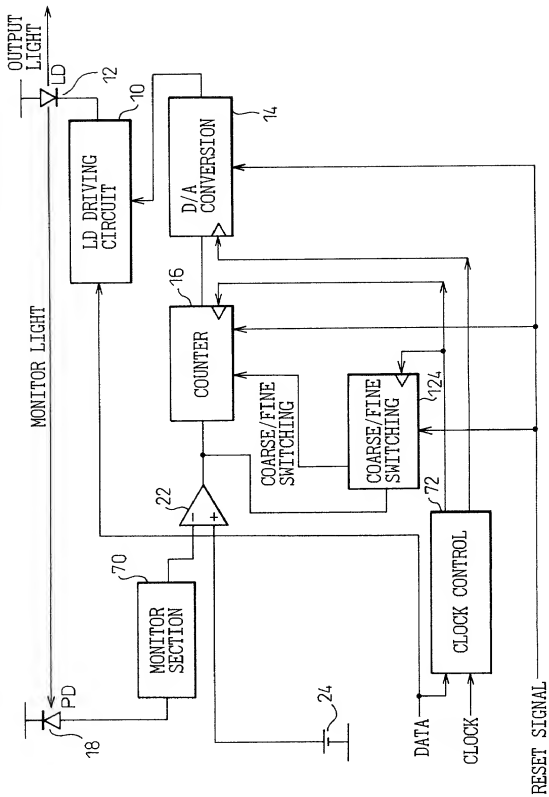


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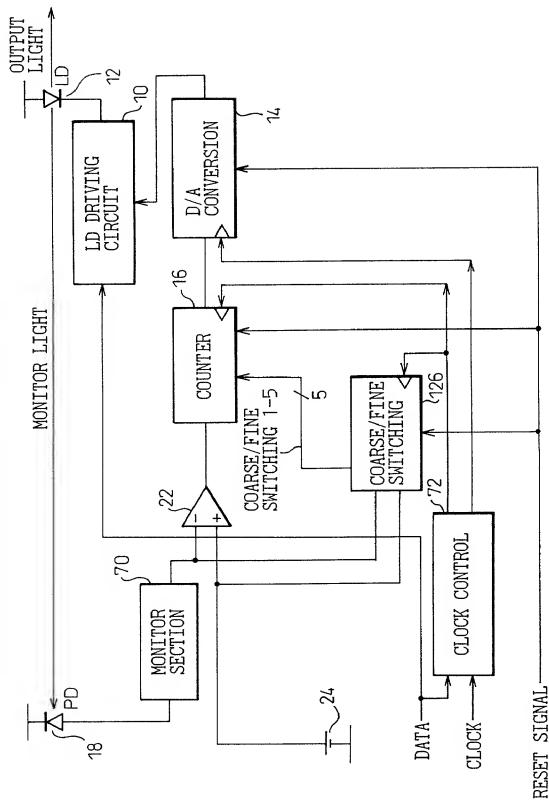


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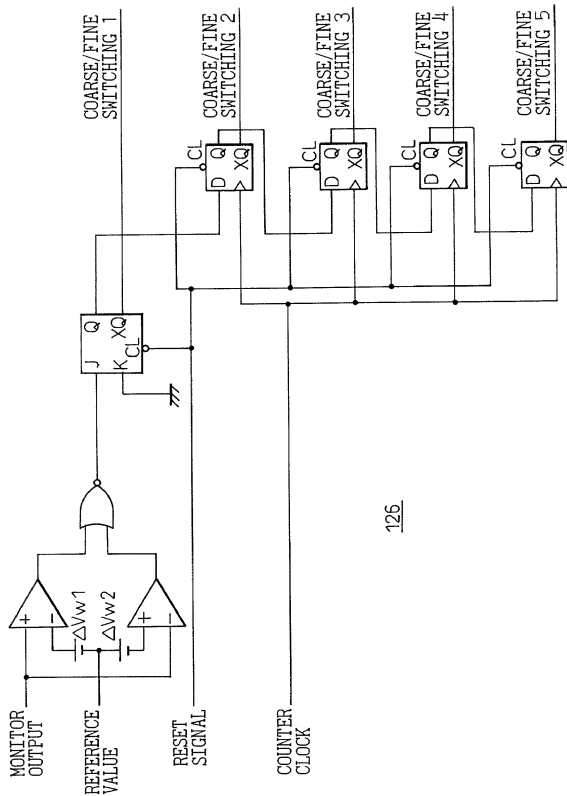


Fig. 44

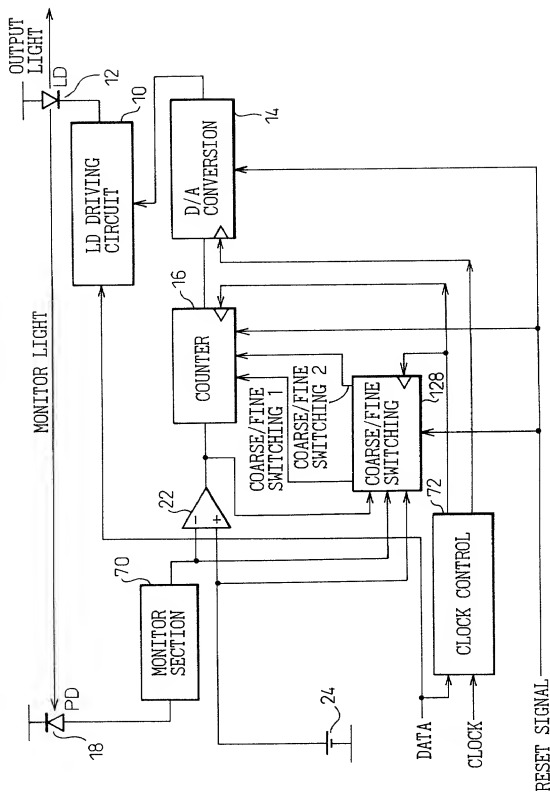
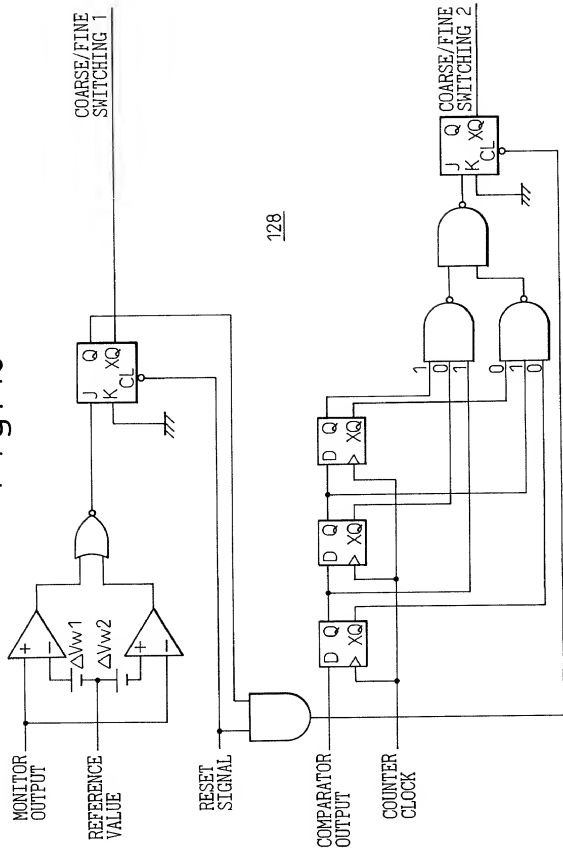


Fig. 45



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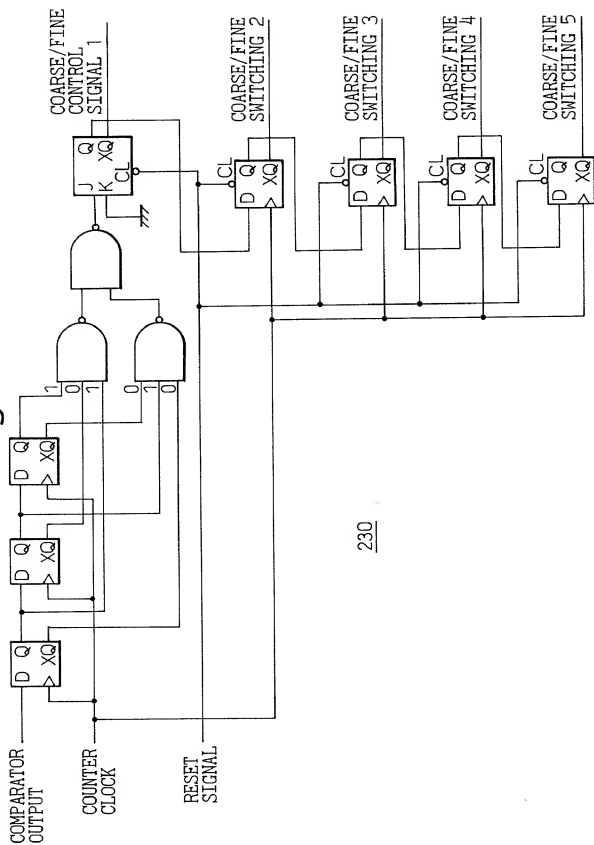


Fig. 47

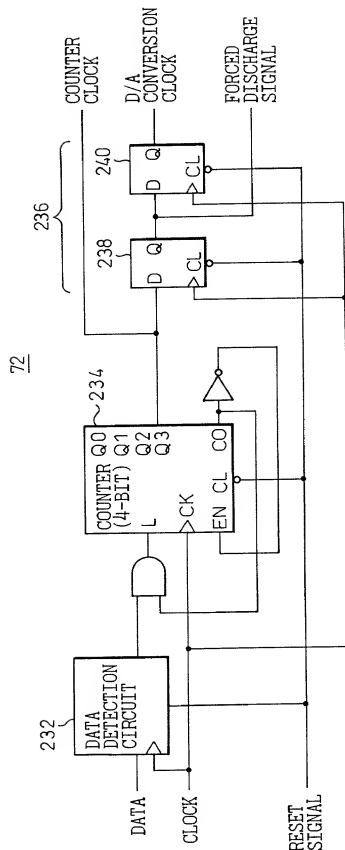
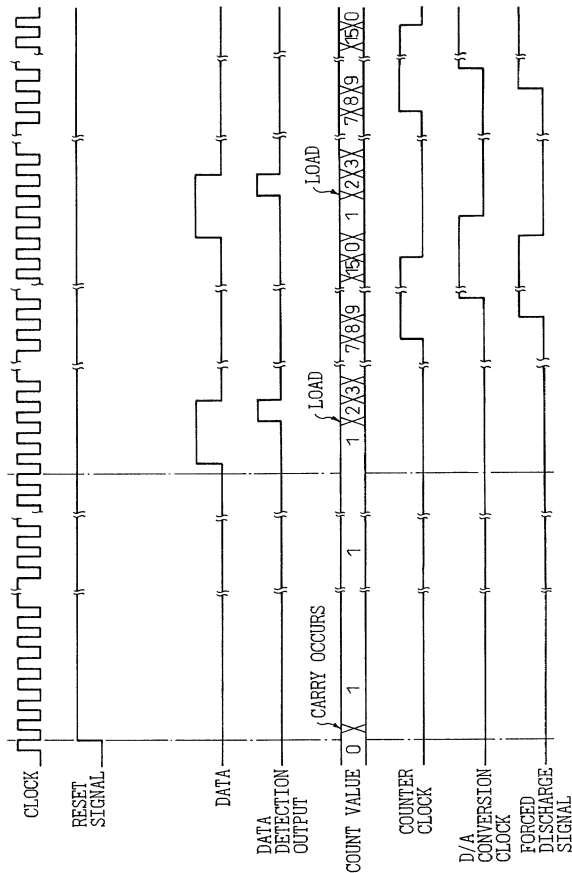
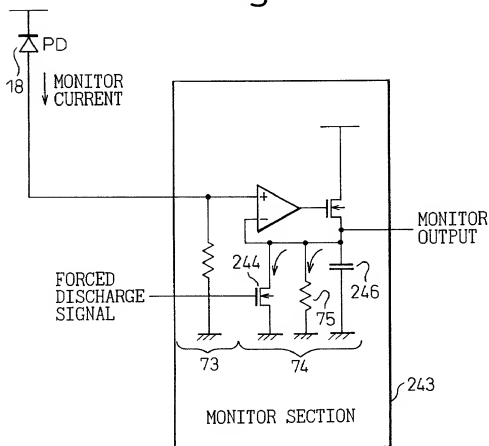


Fig. 48



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OUTPUT OF
COMPARATOR 22

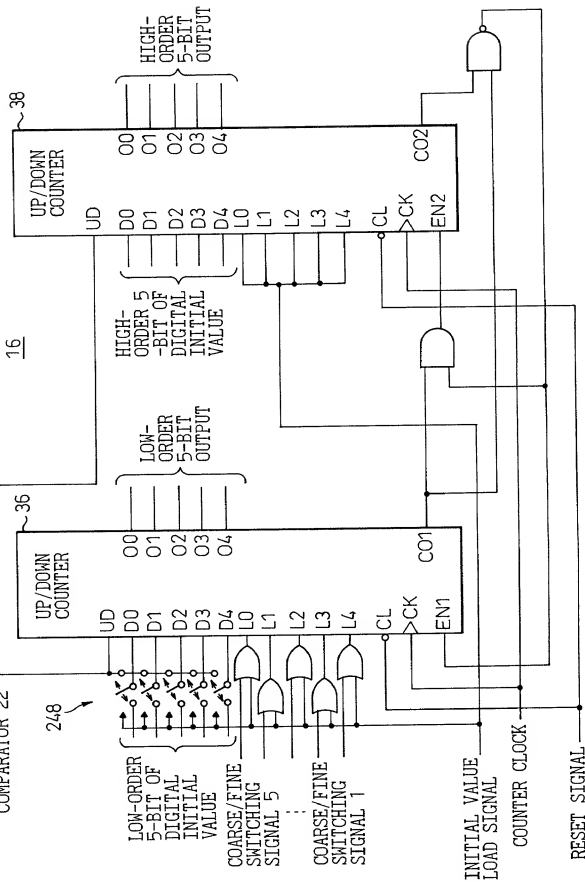


Fig. 52

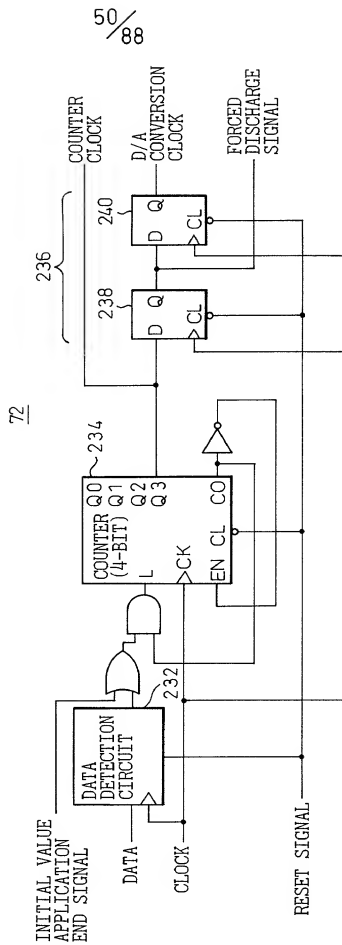


Fig. 53

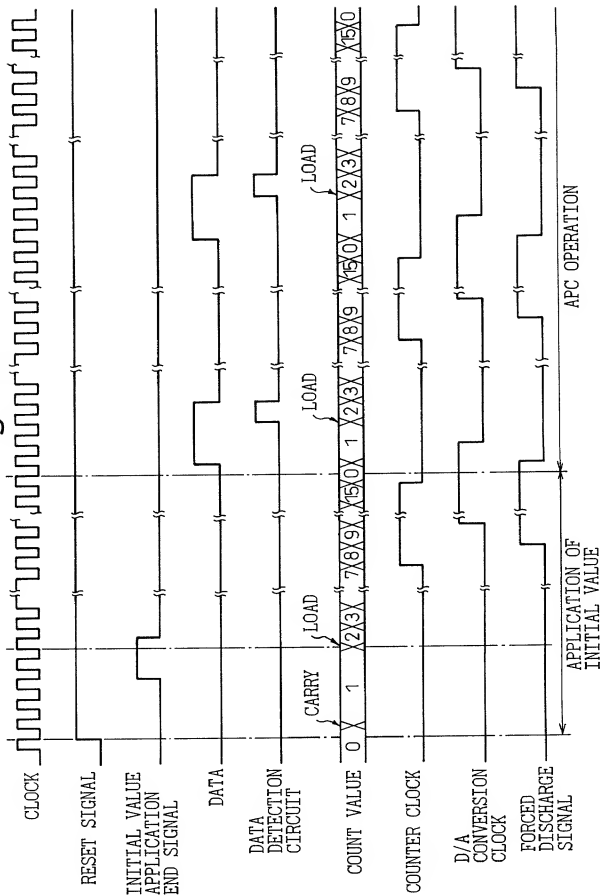


Fig. 54

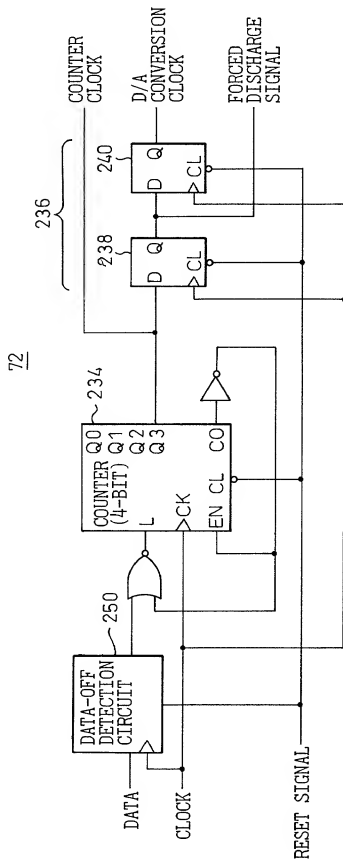


Fig.55

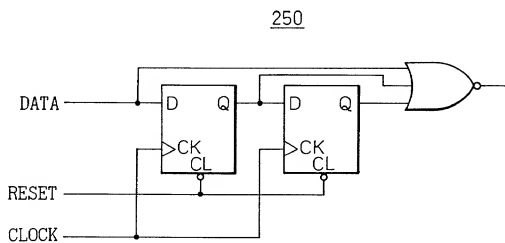


Fig. 56

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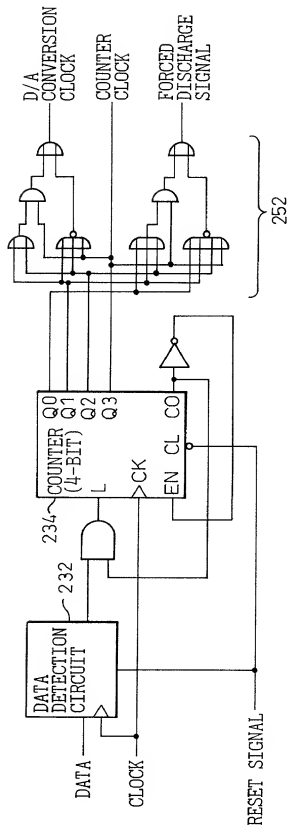


Fig. 58

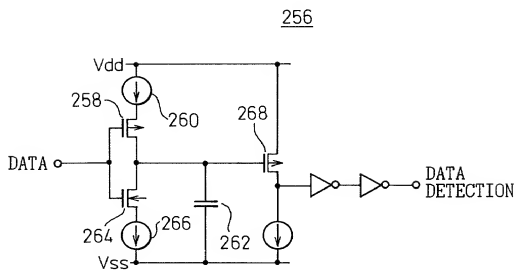
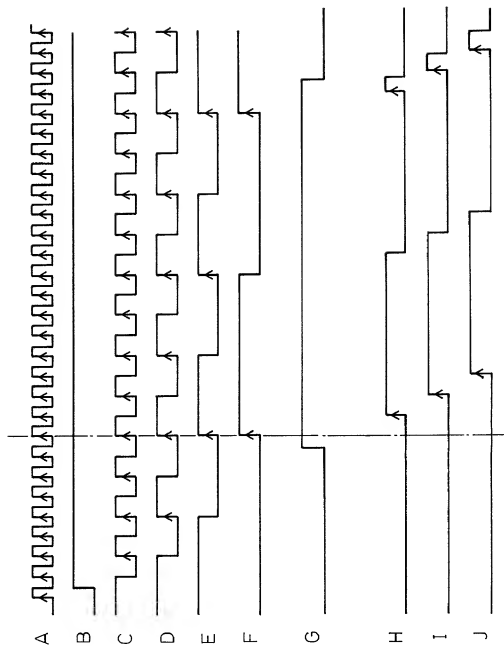


Fig. 59



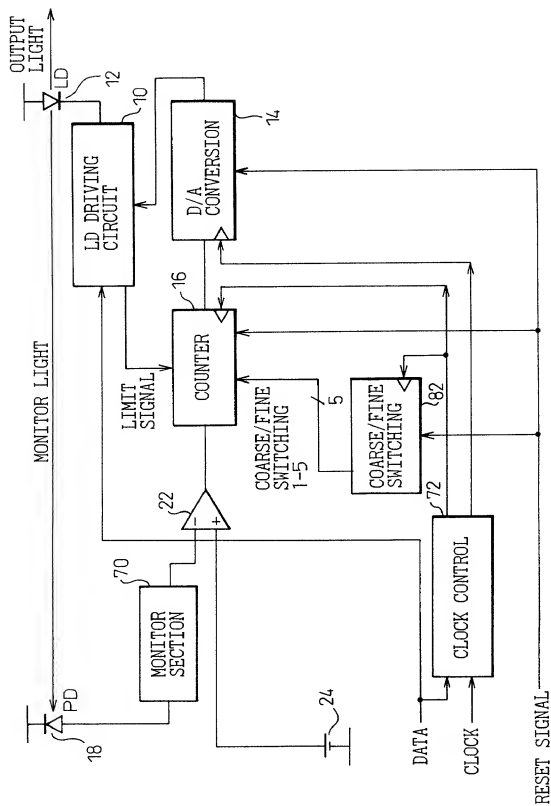
[illegible]

Fig. 62

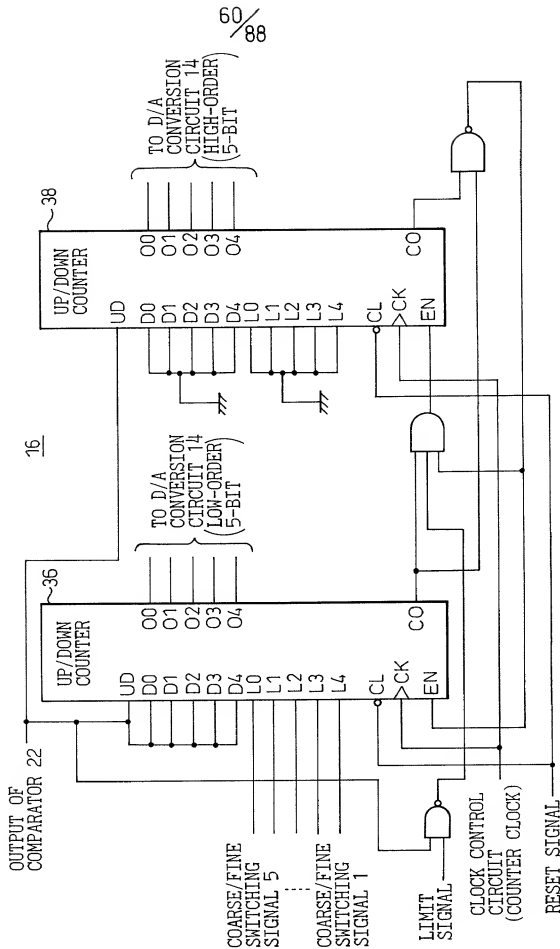


Fig. 63

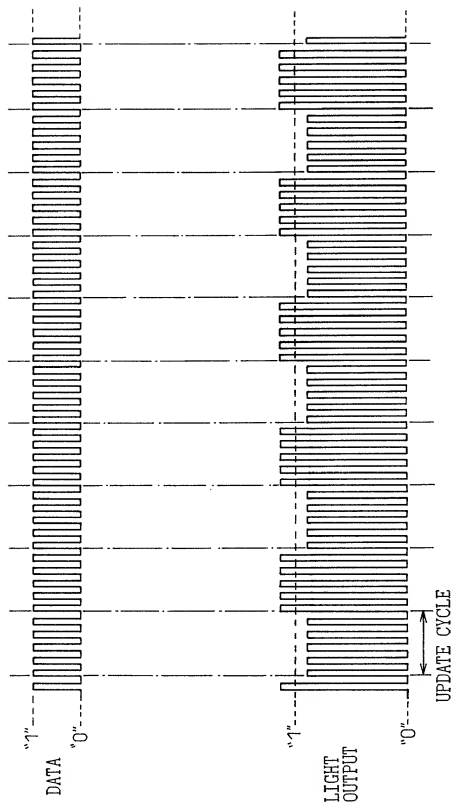
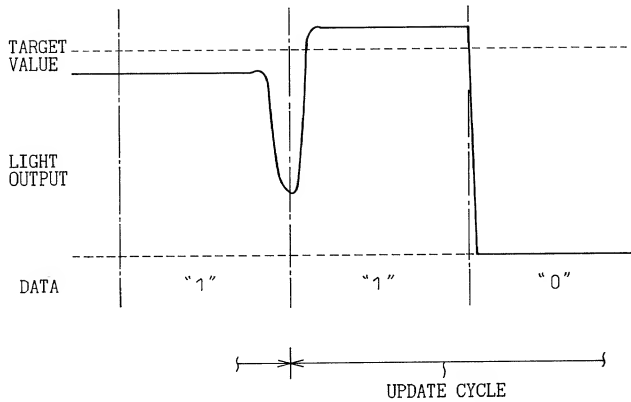


Fig.64



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Fig. 65

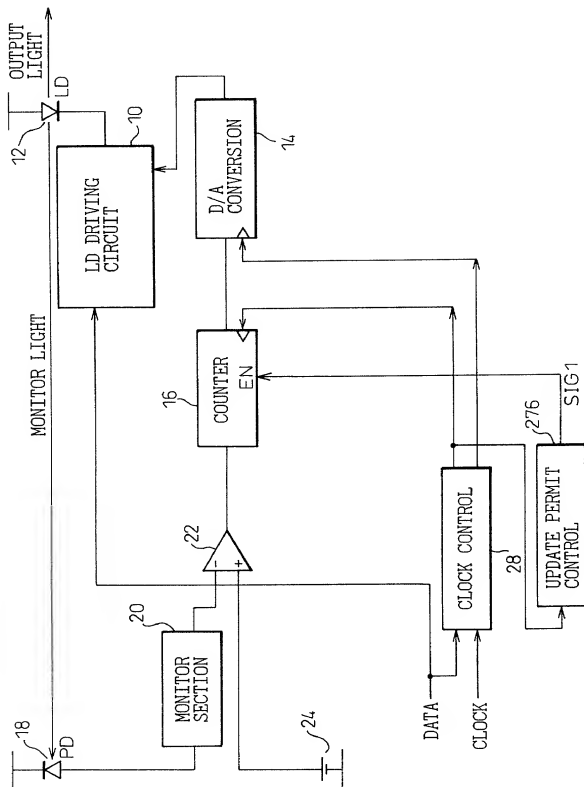


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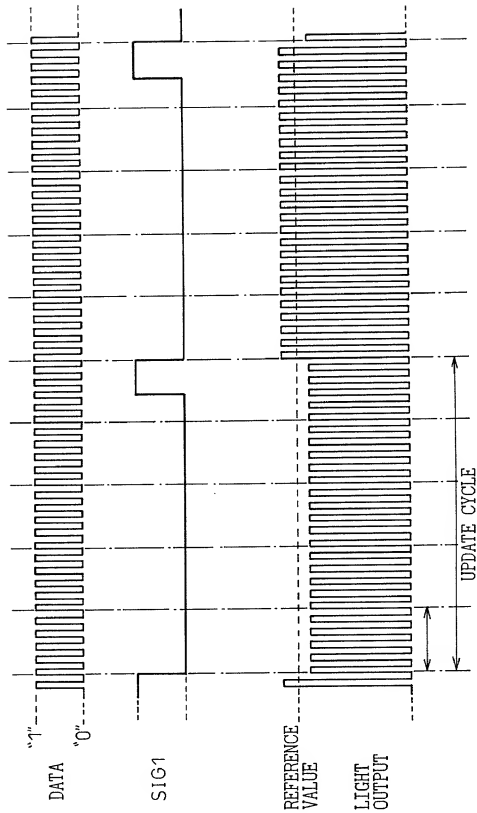


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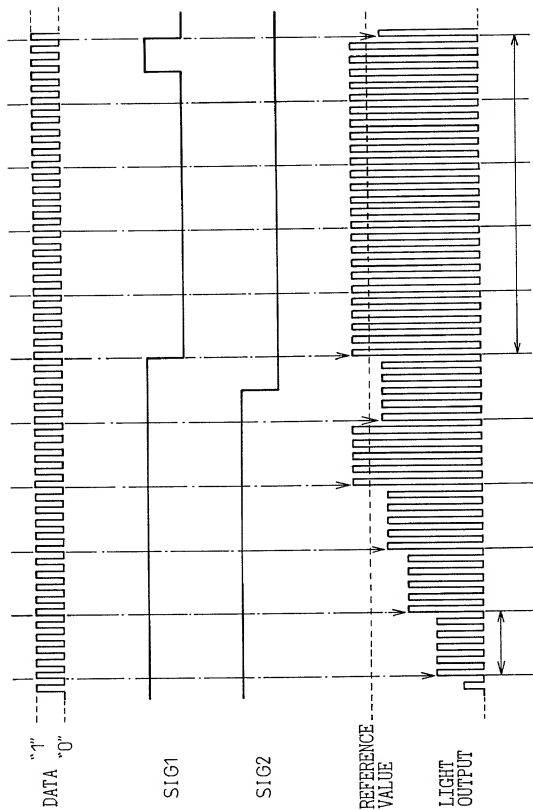


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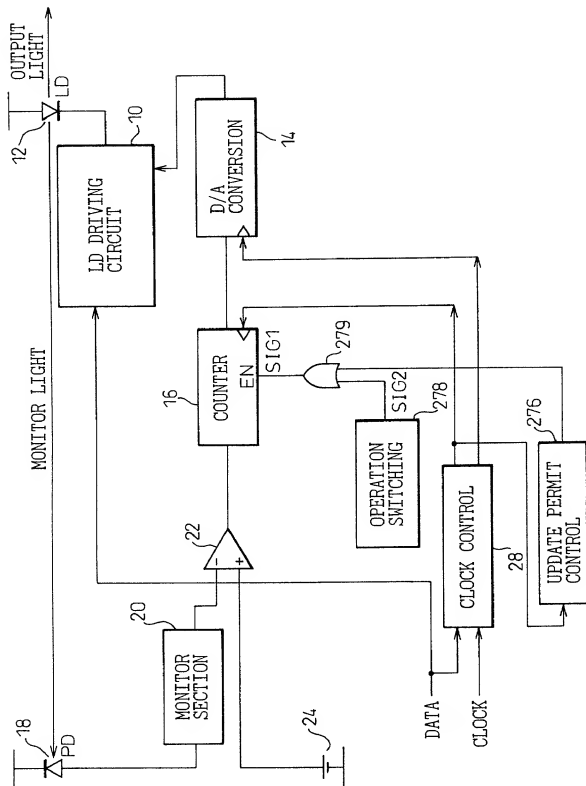


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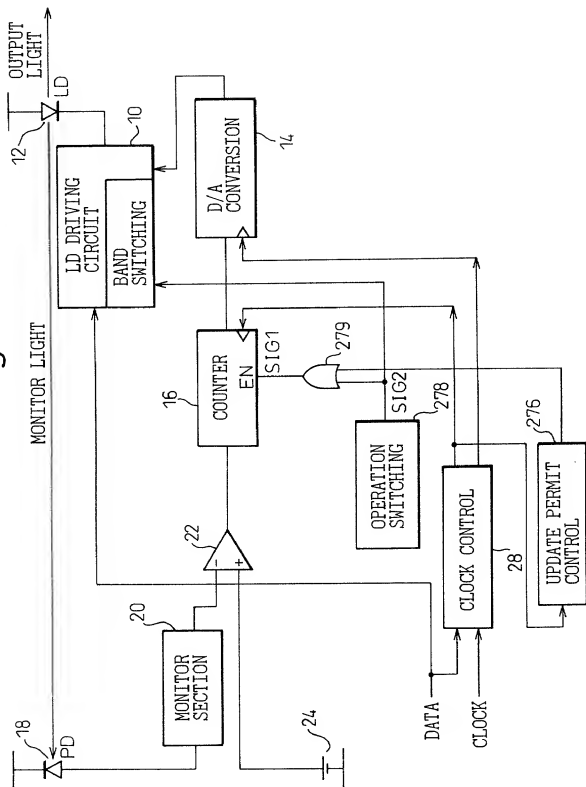


Fig.70

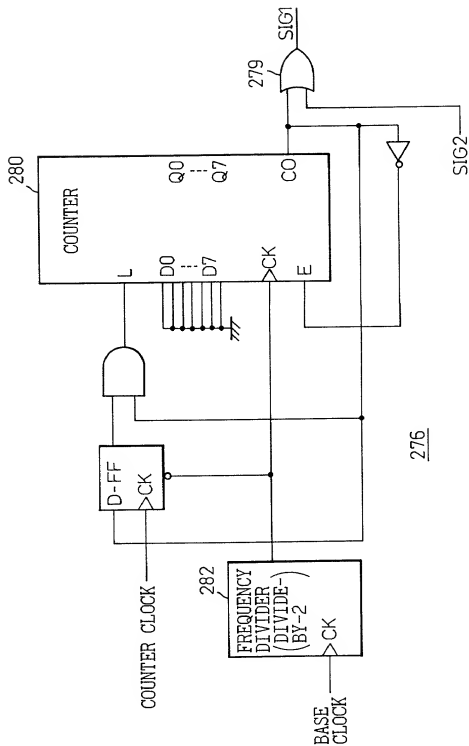


Fig. 72

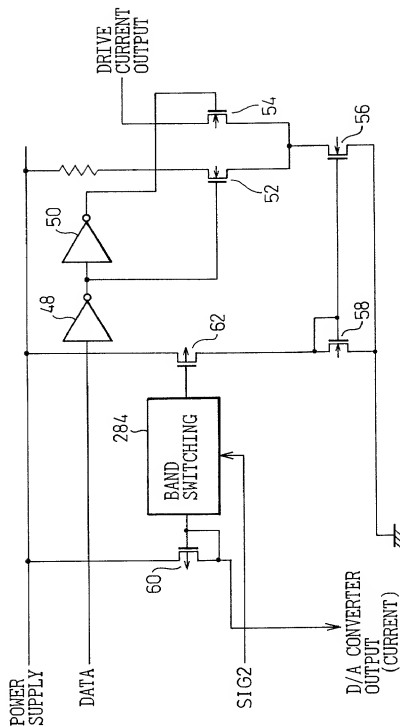


Fig. 73

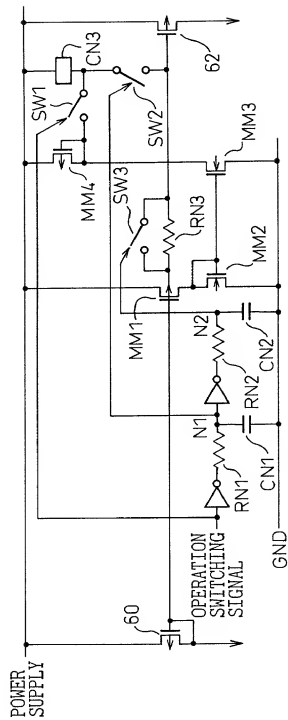


Fig. 74

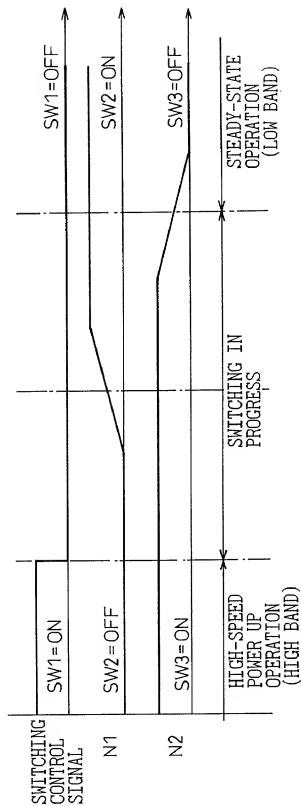


Fig.75

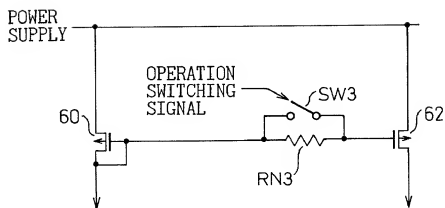


Fig.76

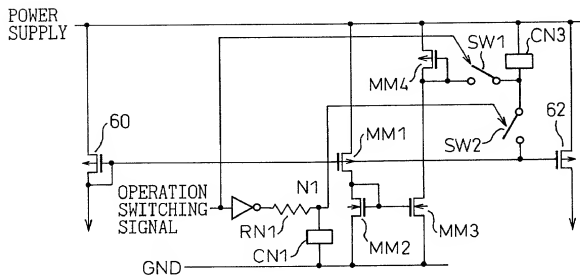


Fig. 77

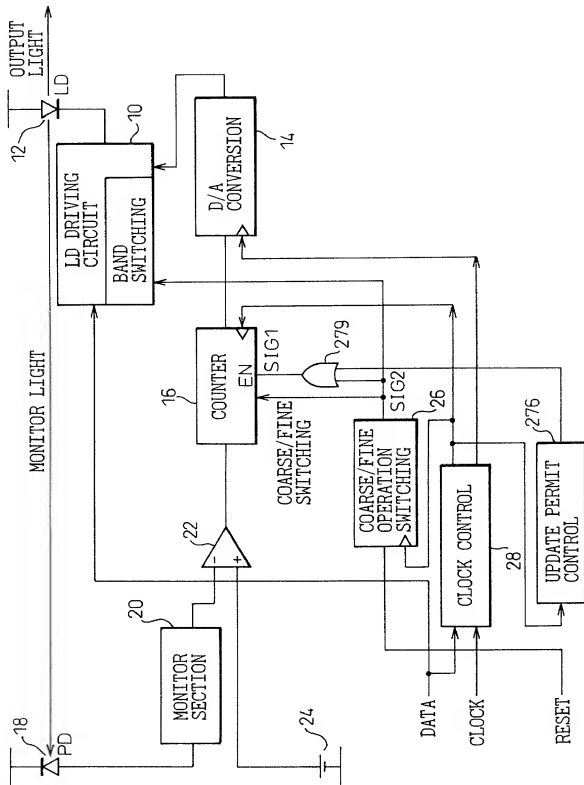


Fig. 78

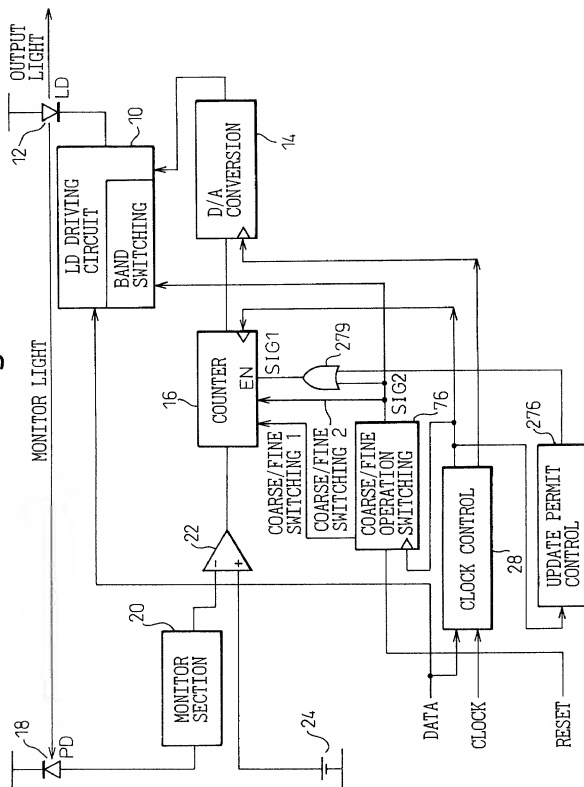


Fig. 79

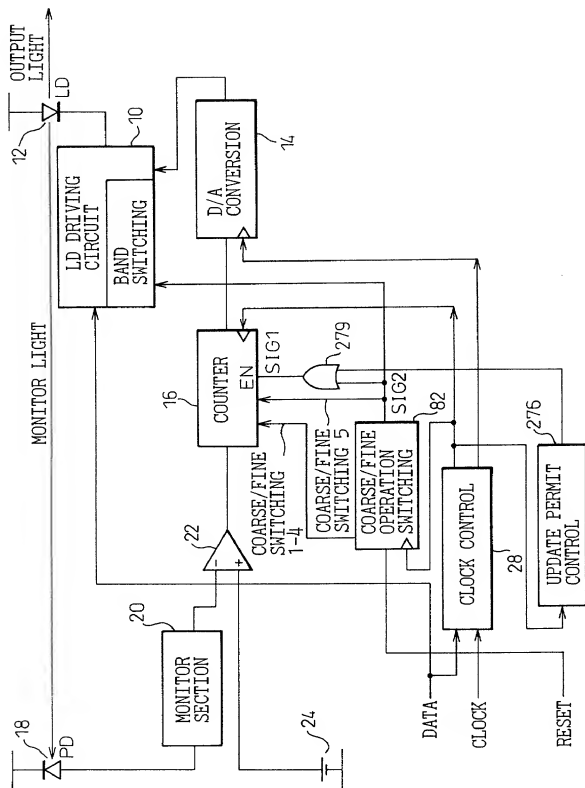


Fig. 80

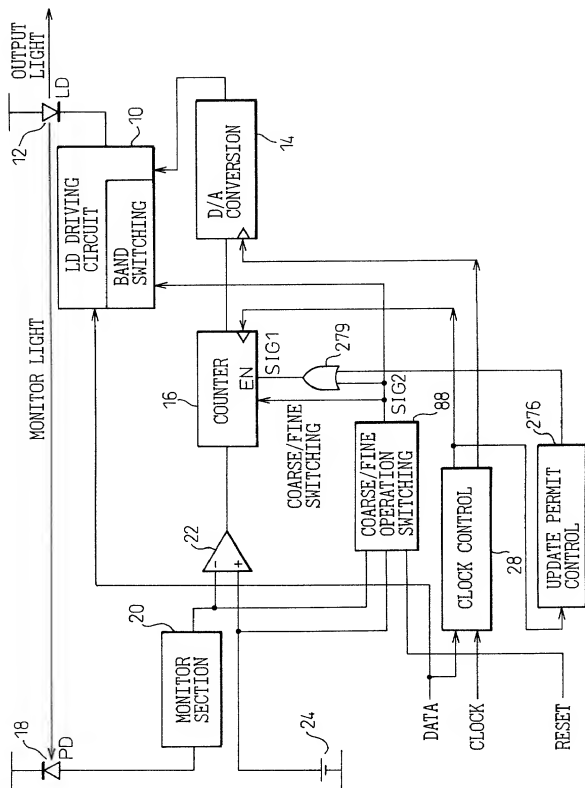


Fig. 81

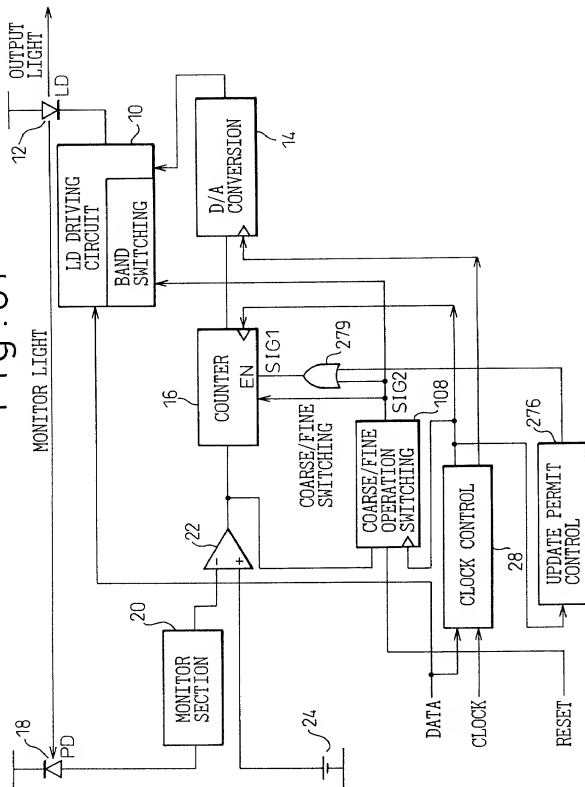


Fig. 82

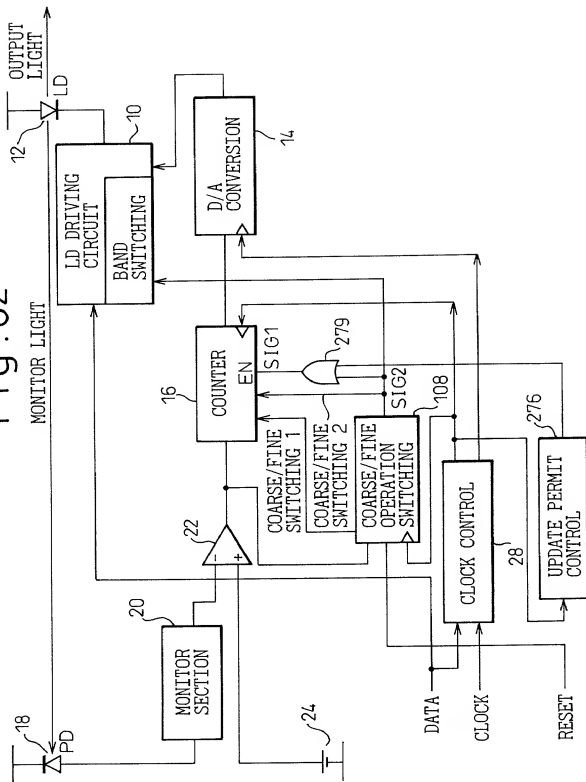


Fig. 83

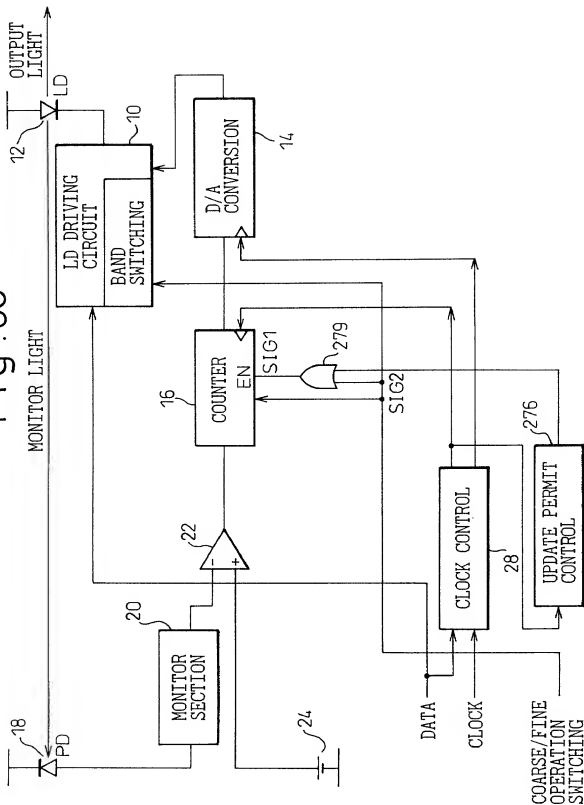


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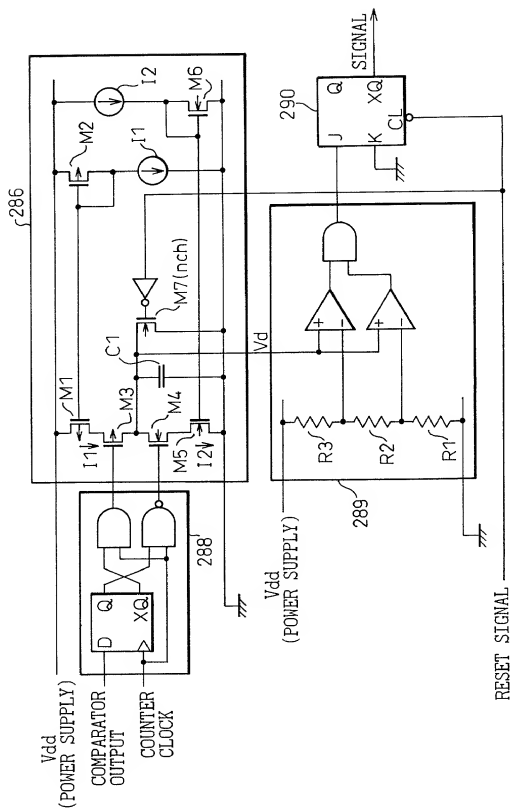


Fig. 85

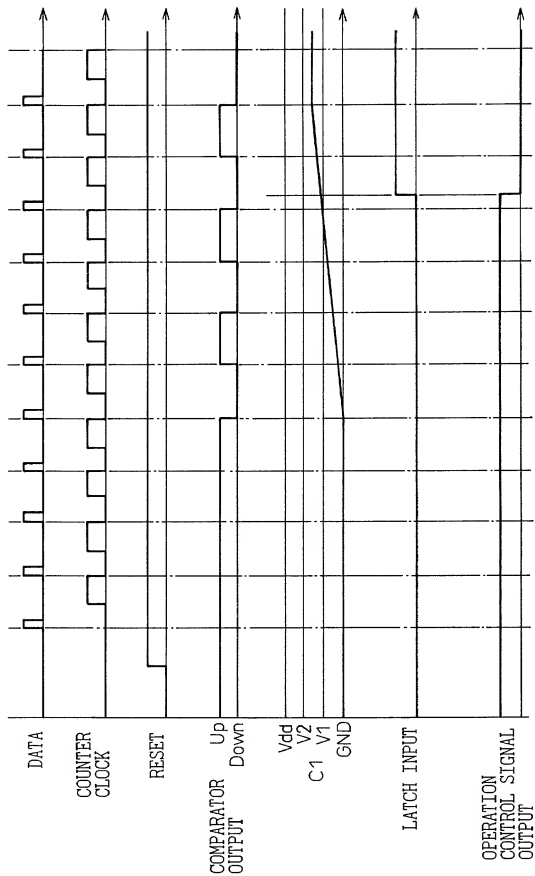


Fig. 86

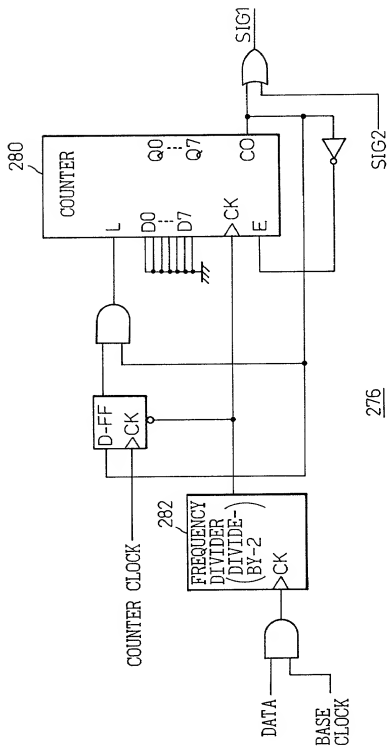


Fig.87

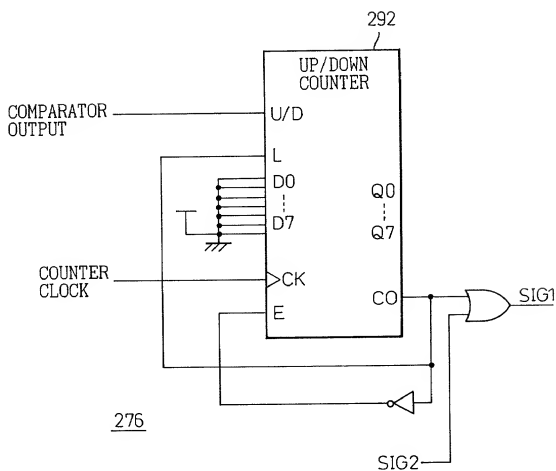
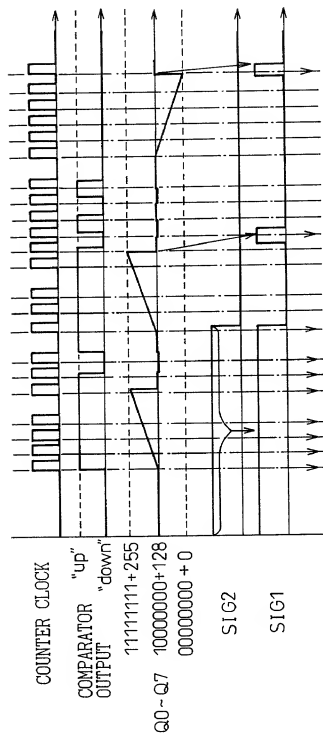


Fig. 88



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Fig.90

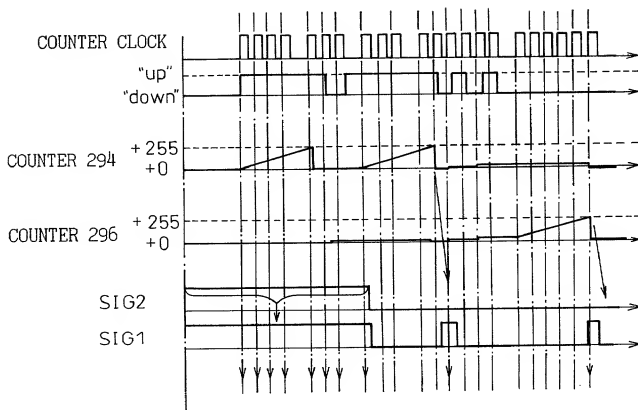


Fig.91

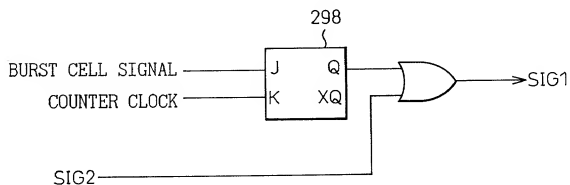
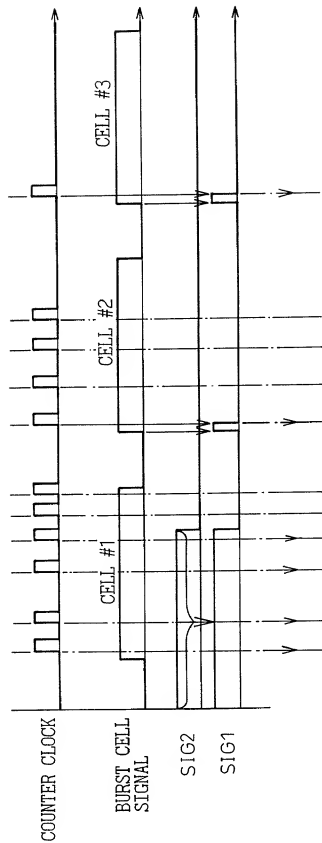


Fig. 92



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Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

LIGHT OUTPUT CONTROL CIRCUIT

上記発明の明細書（下記の欄でx印がついていない場合は、本書に添付）は、

the specification of which is attached hereto unless the following box is checked:

☐ 月 日に提出され、米国出願番号または特許協定条約国際出願番号を _____ とし、
（該当する場合） _____ に訂正されました。

☐ was filed on _____
as United States Application Number or
PCT International Application Number
_____ and was amended on _____
(if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第37編第1章56項に定義されるとおり、特許資格の権利について重要な開示を明示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

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Japanese Language Declaration

(日本語宣言書)

私は、米国法典第35編119条(a)-(d)項又は365条(b)項に基づき下記の、米国以外の国の少なくとも一ヶ国を指定している特許協力条約365(a)項に基づき国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

Prior Foreign Application(s)

外国での先行出願

11-042178 (Pat. Appln.) Japan

(Number)

(Country)

(番号)

(国名)

(Number)

(Country)

(番号)

(国名)

私、第35編米国法典119条(e)項に基づいて下記の米国特許出願規定に記載された権利をここに主張いたします。

(Application No.)

(出願番号)

(Filing Date)

(出願日)

私は、下記の米国法典第35編120条に基づいて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約365条(c)に基づき権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第35編112条第1項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入乎された、連邦規則法典第37編1.56条5項で記載された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

(Application No.)

(出願番号)

(Filing Date)

(出願日)

(Application No.)

(出願番号)

(Filing Date)

(出願日)

私は、私自身の知識に基づいて本宣言書で私が行なう表明が真実であり、かつ私の入手した情報と私の信じることに基づき表明が全て真実であると信じていること、さらに放棄なられた虚偽の表明及びそれと同等の行為は米国法典第18編第1001条に基づき、罰金または有罪、もしくはその両方により処罰されること、そしてそのような虚偽による虚偽の表明を行なえば、出願した、又は更に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT international application having a filing date before that of the application on which priority is claimed.

Priority Not Claimed

優先権主張なし

19/February/1999

(Day/Month/Year Filed)

(出願年月日)

(Day/Month/Year Filed)

(出願年月日)

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.)

(出願番号)

(Filing Date)

(出願日)

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT international application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of application.

(Status: Patented, Pending, Abandoned)

(状況: 特許許可済、係属中、放棄済)

(Status: Patented, Pending, Abandoned)

(状況: 特許許可済、係属中、放棄済)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Japanese Language Declaration

(日本語宣言書)

委任状: 私は下記の発明者として、本出願に関する一切の
手続を米特許庁長官に対して遂行する弁護士または代理人
として、下記の者を指名いたします。(弁護士、または代理
人氏名及び登録番号を明記のこと)

POWER OF ATTORNEY: As a named inventor, I hereby appoint
the following attorney(s) and/or agent(s) to prosecute this
application and transact all business in the Patent and Trademark
Office connected therewith (list name and registration number)

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William F. Herbert, 31,024; Richard A. Gollhofer, 31,106; Mark J. Henry, 36,162; Gene M. Garner II, 34,172; Michael D. Stein, 37,240; Paul
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唯一または第一発明者名	Full name of sole or first inventor
Tadao Inoue	
発明者の署名	Inventor's signature
日付	Date
井上 達夫	February 10, 2000
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国籍	Citizenship
Japanese	
私書箱	Post Office Address
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第二共同発明者	Full name of second joint inventor, if any
Tadashi Ikeuchi	
第二共同発明者	Second inventor's signature
日付	Date
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住所	Residence
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(第三以降の共同発明者についても同様に記載し、署名をする
こと)

(Supply similar information and signature for third and subsequent
joint inventors.)

第三共同発明者	Full name of third joint inventor, if any Hiroyuki Rokugawa
第三共同発明者 日付	Third inventor's signature Date <i>Hiroyuki Rokugawa</i> February 10, 2000
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第五共同発明者	Full name of fifth joint inventor, if any Norio Ueno
第五共同発明者 日付	Fifth inventor's signature Date <i>Norio Ueno</i> February 10, 2000
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第六共同発明者	Full name of sixth joint inventor, if any Norio Murakami
第六共同発明者 日付	Sixth inventor's signature Date <i>Norio Murakami</i> February 10, 2000
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(第七以降の共同発明者についても同様に記載し、署名をすること)

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第七共同発明者		Full name of seventh joint inventor, if any Toru Matsuyama
第七共同発明者	日付	Seventh inventor's signature Date <i>Toru Matsuyama</i> February 10, 2000
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第八共同発明者		Full name of eighth joint inventor, if any Makoto Miki
第八共同発明者	日付	Eighth inventor's signature Date <i>Makoto Miki</i> February 10, 2000
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第九共同発明者		Full name of ninth joint inventor, if any Toshiyuki Takauji
第九共同発明者	日付	Ninth inventor's signature Date <i>Toshiyuki Takauji</i> February 10, 2000
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第十共同発明者		Full name of tenth joint inventor, if any
第十共同発明者	日付	Tenth inventor's signature Date
住 所		Residence
国 籍		Citizenship
私書箱		Post Office Address

(第十一以降の共同発明者についても同様に記載し、署名をすること)

(Supply similar information and signature for eleventh and subsequent joint inventors.)